Compal LA-L931P

V350-ADL MB Schematic Document

Rev: 1.0

2021.10.12

Security Classification	Compal Secret Data		
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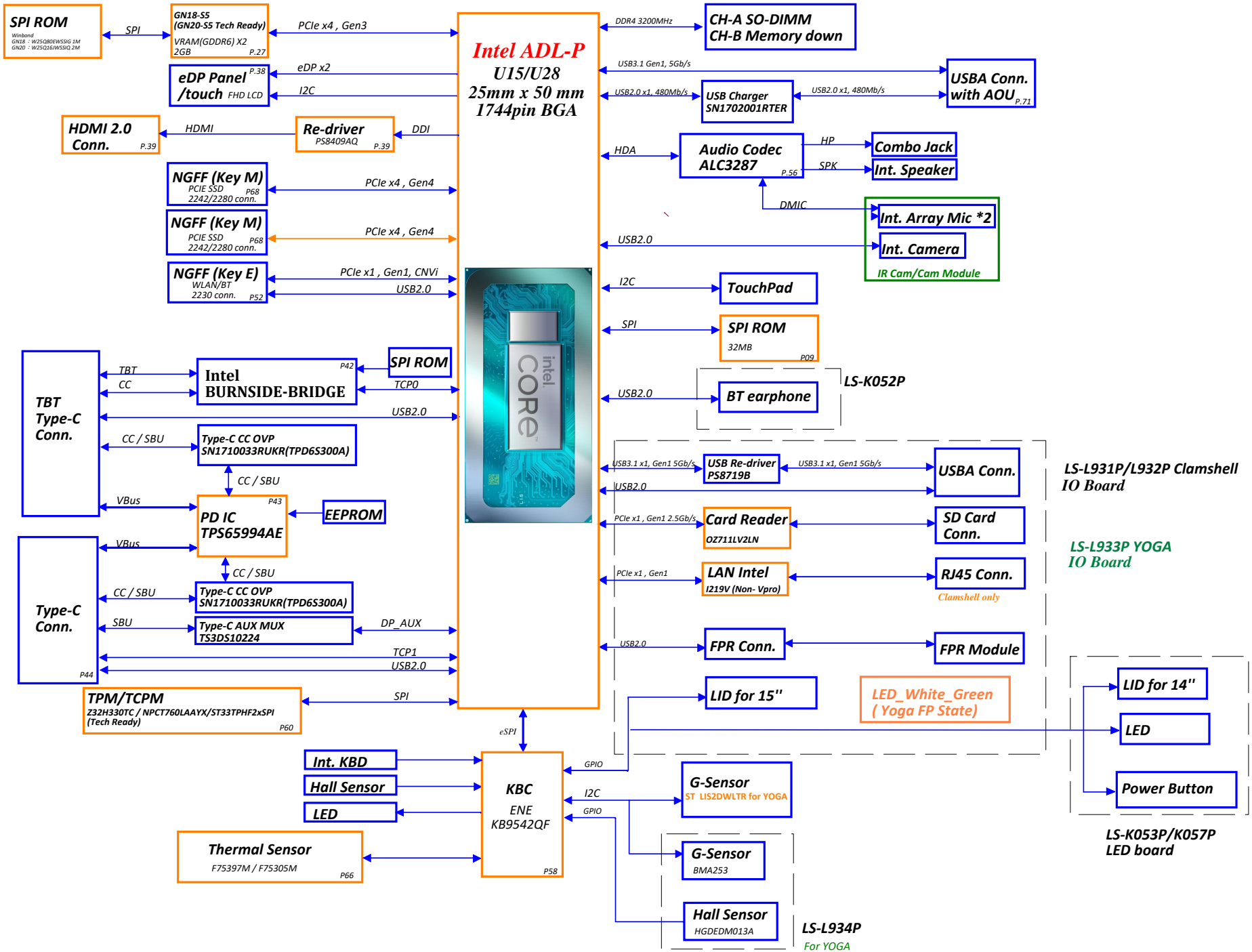
Title: *Cover Sheet EE*		
Size	Document Number: *LA-L931P*	Rev: 1.0
Date: Tuesday, January 25, 2022	Sheet 1 of 120	



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			ADL-P Block Diagrams EE
			LA-L931P

BOM Structure Table

Function	Stuff	Un-Stuff
dGPU SKU	DIS@	UMA@
YOGA SKU	YOGA@	CLAMSHELL@
CLAMSHELL SKU	CLAHSHELL@	YOGA@
DDR DDP	DDP@	SDP@
DDR SDP	SDP@	DDP@
EMI / ESD / RF Components	EMI@ RF@ ESD@ BT_EMI@	@EMI@ @RF@ @ESD@
CNVI	CNVi@	RMT@
USBA AOU	AOU@	NAOU@
TPM	TPM@ ST@ /Nuvton@/ Nations@	NTPM@
KB Backlight	KBL@	
Touch Screen	TOUCH@	NonTOUCH@
For Signal Test	MP@	
BT earphoen	BT@	
Finger Print	FP@	NFP@
NC Components	@	
ME Cnnector	ME@ CLIP@	
JUMP (HW & PWR)	JUMP@	@JUMP@
CPU_ID0	U15@	U28@
TBT	TBT@	
HDMI	HDMI@	

HSIO Port Table (CPU)

HSIO Port	Capable	Port Allocation	PCIE CLK	NOTE
0	PCIe4_A_#0	SSD1 (Main)	CLK0 & CLKREQ#0	PCIe interface
1	PCIe4_A_#1			
2	PCIe4_A_#2			
3	PCIe4_A_#3			
4	PCIe4_B_#0	SSD2 (Second)	CLK0 & CLKREQ#3	PCIe interface
5	PCIe4_B_#1			
6	PCIe4_B_#2			
7	PCIe4_B_#3			

USB2.0 Port Table

USB2.0 Port	Device
1	USB Type-A (MB)
2	USB Type-C (MB TBT)
3	USB Type-C (MB)
4	USB Type-A (DB)
5	Camera
6	Finger print
7	NA
8	BT earphone
9	NA
10	NGFF_BT

HSIO Port Table (PCH)

HSIO Port	Capable	Port Allocation	PCIE CLK	NOTE
0	USB3.1 #1 / PCIe #1	USB3.1 Type A Port 1 (MB)	NA	USB3.1 interface
1	USB3.1 #2 / PCIe #2	USB3.1 Type A Port 2 (DB)	NA	USB3.1 interface
2	USB3.1 #3 / PCIe #3	WLAN	CLK5 & CLKREQ#5	PCIe interface
3	USB3.1 #4 / PCIe #4	USB3.1 Type A Port 2 (DB)	NA	USB3.1 interface
4	PCIe #5	DGPU	CLK4 & CLKREQ#4	PCIe interface
5	PCIe #6			
6	PCIe #7			
7	PCIe #8			
8	PCIe #9	LAN	CLK1 & CLKREQ#1	PCIe interface
9	PCIe #10	Carder Reader	CLK2 & CLKREQ#2	PCIe interface
10	PCIe #11 /SATA0			
11	PCIe #12 /SATA1			

Power State

STATE \ SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
S0IX	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

Load BOM Option Table

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	
431ACX30L02(UMA)	

Load BOM Option Table for Baseline

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	
431ACX30L02(UMA)	

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SOC_SMBCLK SOC_SMBDATA	+3V_PRIM	DIMM1	TBC	TBC	0xA0
		DIMM2	TBC	TBC	0xA4
SOC_SML0CLK_R SOC_SML0DATA_R	+3V_PRIM	Re-Timer	TBC	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3VALW	PD (TI65994)	TBC	TBC	TBC
		PD (CYPD5225)	0x08h	TBC	TBC
TBC	TBC	INTEL LAN	TBC	TBC	0xC8

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
EC_SMB_CK1 EC_SMB_DA1	+3VL	BAT	0x16	TBC	TBC
		CHGR	0x12	TBC	TBC
EC_SMB_CK2 EC_SMB_DA2	+3VL	GPU	0x41	TBC	TBC
		THERMAL	0x4C	0X98	0x99
		PD (CYPD5225)	0x08h	TBC	TBC
		PD (TI65994)	TBC	0X46	0X47
				0X4E	0X4F

I2C Address Table (TBC)

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C 0	+3VS	G-Sensor KXCJ9-1008	0x0FH	TBC	TBC
		ALS CM32181A3OP	0x48H	TBC	TBC
I2C 2	+3VS	HDMI2.0 Re-Timer	TBC	TBC	TBC
I2C 3	+3VS	Track Pad	0x2CH	TBC	TBC
ISH_I2C 0	+1.8VS	SENSOR_KMX61G (Reserve)	0FH	TBC	TBC

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5
+20V_ADP_IN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+1.0VS_DGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VCCPLL_OC	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.2V_VDDQ	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF
+2.5V	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF					

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Size	Document Number		Rev
	LA-L931P		1.0
Date:	Tuesday, January 25, 2022	Sheet	3 of 120

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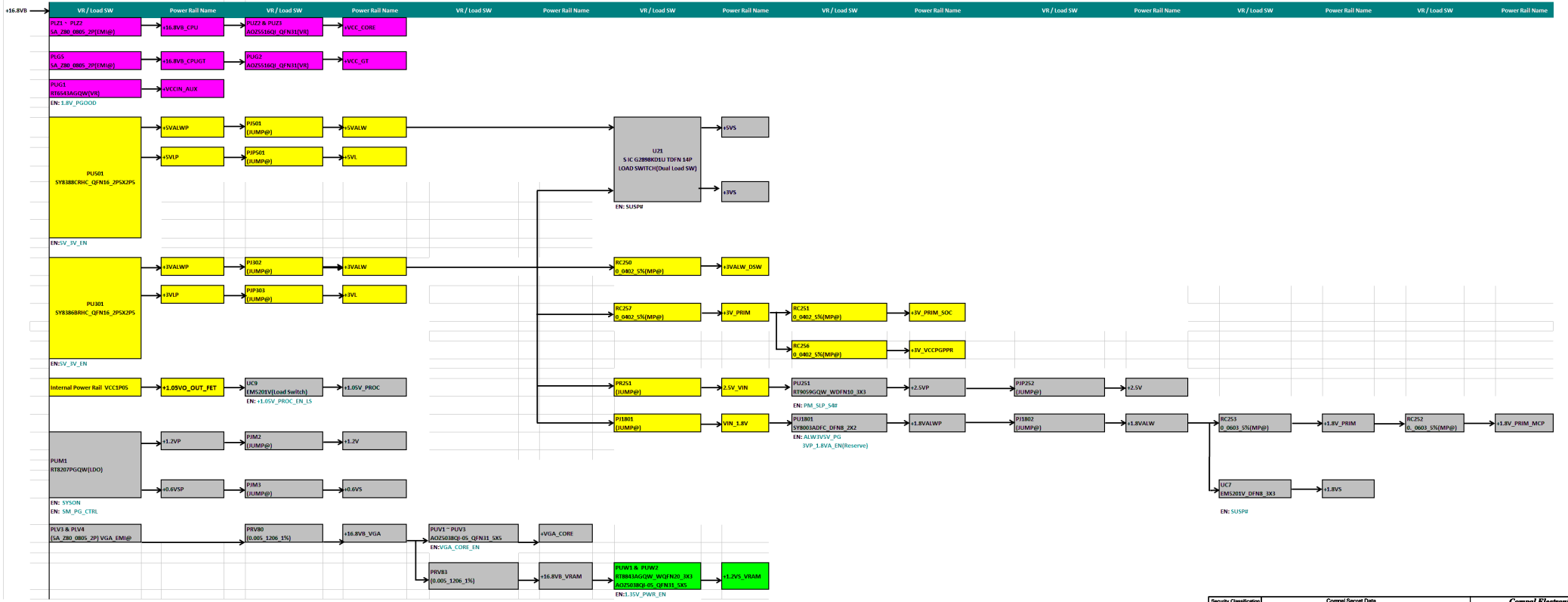
[HLXA4_A5-Power Map_ADL-P_DDR4]

XA4/5 Schemat LA-L931P01_0702A



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			Date: Tuesday, January 25, 2022 Sheet 4 of 135

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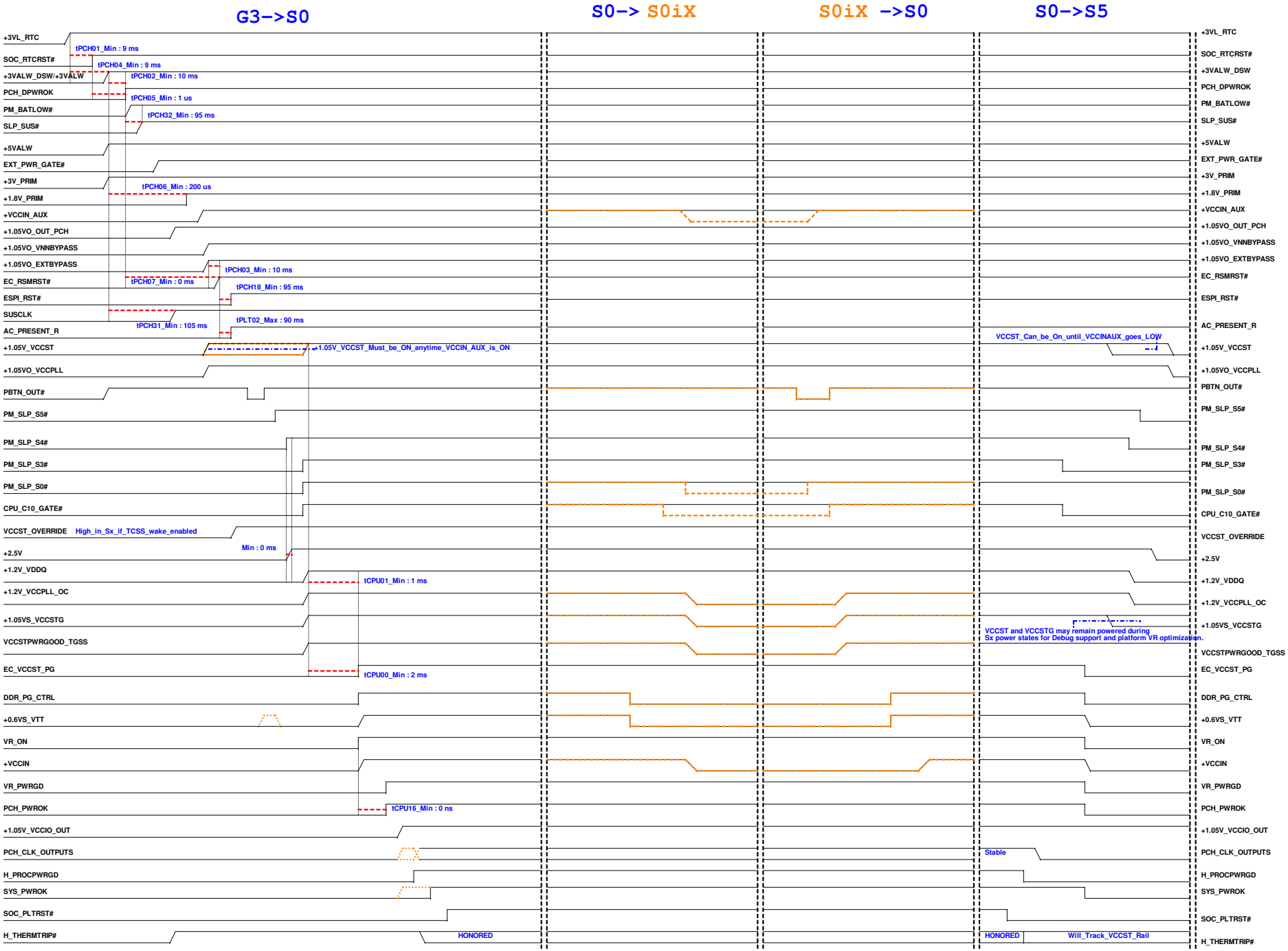
[FQA01-PWR Sequence_TGL-UP3_DDR4_Volume_S0iX]

Will be Update



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Size	Document Number: LA-L931P		Rev: 1.0
Date: Tuesday, January 25, 2022	Sheet 5 of 120		

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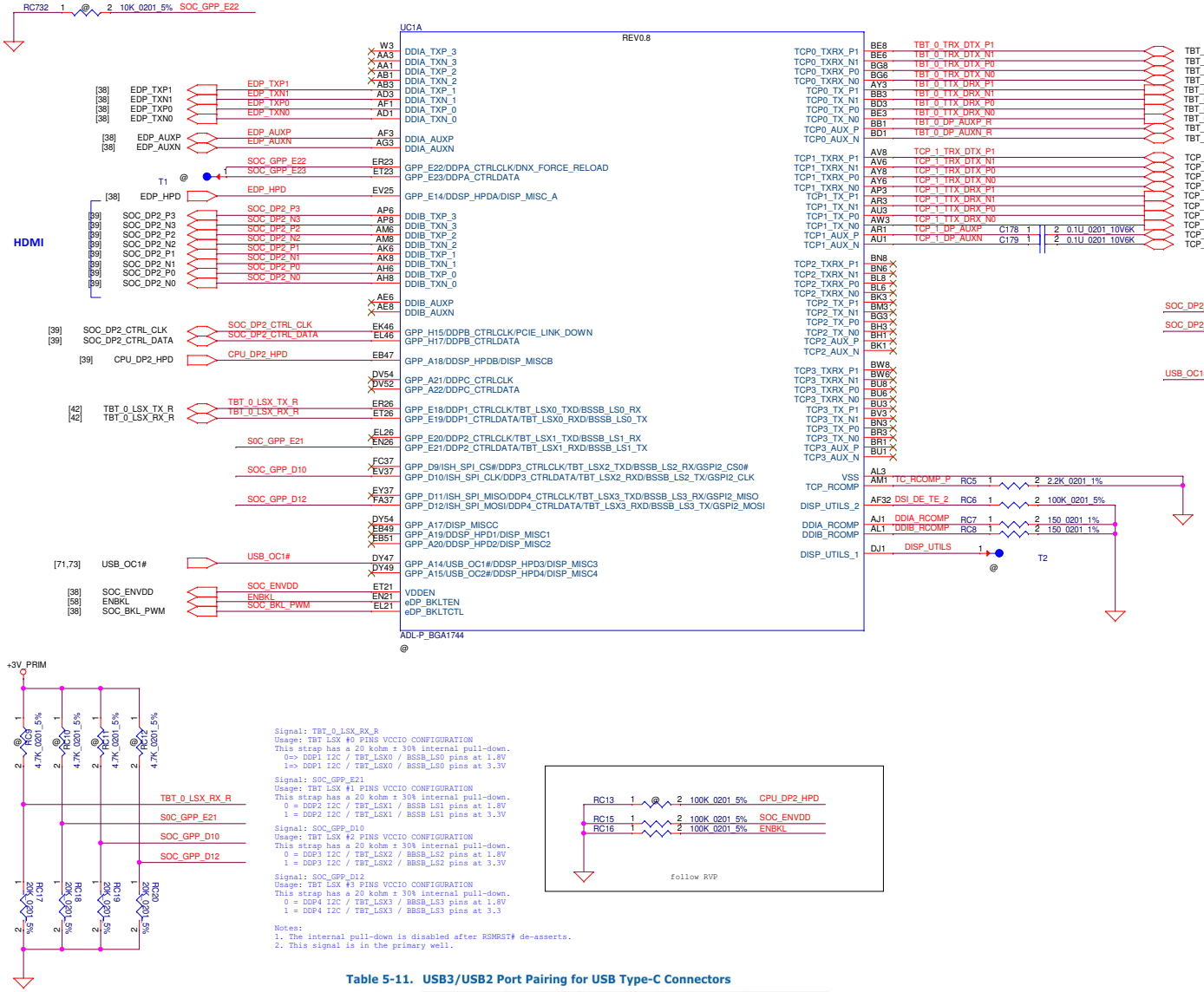

CPU config.

28W

UC1 — SRLD6
SA0000FBV30
S IC FJ80715047866O7 SRLD6 L0 2.1G FCBGA 1744 C38 !
28W_i7@

UC1 — SRLD9
SA0000F9F80
S IC FJ80715047879O7 SRLD9 L0 1.7G BGA 1744 C38 !
28W_i5@

UC1 — SRLFY
SA0000FE840
S IC FJ80715048274O2 SRLFY R0 1.5G BGA 1744 C38 !
28W_i3@

Celeron

UC1 — SRLFX
SA0000FE340
S IC FJ80715048273O0 SRLFX R0 1.1G BGA 1744 C38 !
celeron@

15W

UC1 — SRLFP
SA0000FB570
S IC FJ80715048266O7 SRLFP R0 1.7G BGA 1744 C38 !
15W_i7@

UC1 — SRLFQ_w IPU
SA0000FB770
S IC FJ80715048268O2 SRLFQ R0 1.3G BGA 1744 C38 !
15W_i5_w_IPU@

UC1 — SRLFR_w/o IPU
SA0000FE130
S IC FJ80715048268O3 SRLFR R0 1.3G BGA 1744 C38 !
15W_i5_wo_IPU@

UC1 — SRLFT_w IPU
SA0000FBR60
S IC FJ80715048271O0 SRLFT R0 1.2G BGA 1744 C38 !
15W_i3_w_IPU@

UC1 — SRLFU_w/o IPU
SA0000FE250
S IC FJ80715048271O1 SRLFU R0 1.2G BGA 1744 C38 !
15W_i3_wo_IPU@

Signal: TBT_0_LSX_RX_R
Usage: TBT LSX #0 PINS VCCIO CONFIGURATION
This strap has a 20 kohm ± 30% internal pull-down.
0=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 1.8V
1=> DDP1 I2C / TBT_LSX0 / BSSB_LS0 pins at 3.3V

Signal: SOC_GPP_E21
Usage: TBT LSX #1 PINS VCCIO CONFIGURATION
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 1.8V
1 = DDP2 I2C / TBT_LSX1 / BSSB LS1 pins at 3.3V

Signal: SOC_GPP_D10
Usage: TBT LSX #2 PINS VCCIO CONFIGURATION
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 1.8V
1 = DDP3 I2C / TBT_LSX2 / BBSB_LS2 pins at 3.3V

Signal: SOC_GPP_D12
Usage: TBT LSX #3 PINS VCCIO CONFIGURATION
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V
1 = DDP4 I2C / TBT_LSX3 / BBSB_LS3 pins at 3.3

Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

follow RVP

Table 5-11. USB3/USB2 Port Pairing for USB Type-C Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.

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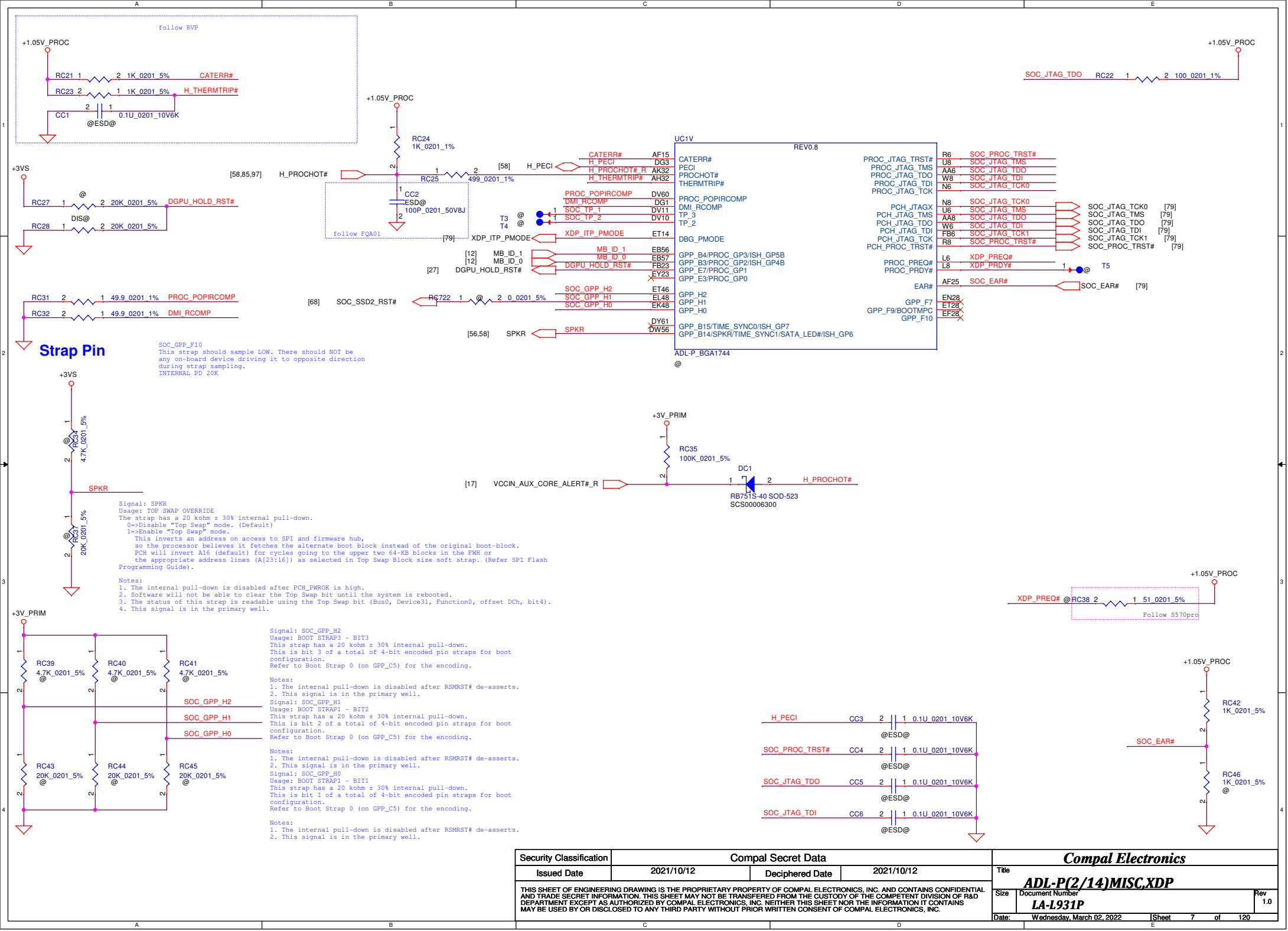
Size	Document Number		Rev
	LA-L931P		1.0
Date:	Wednesday, March 02, 2022	Sheet	6 of 120



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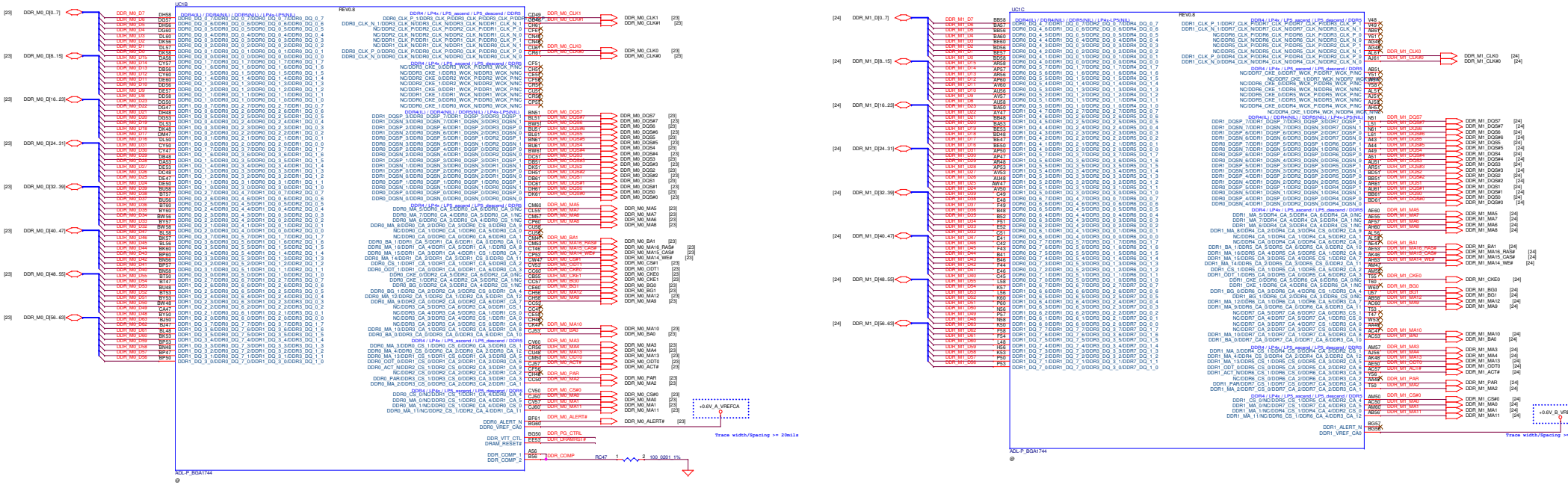
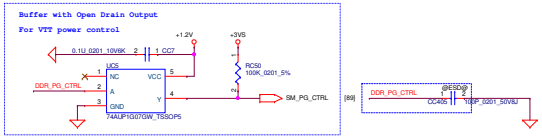
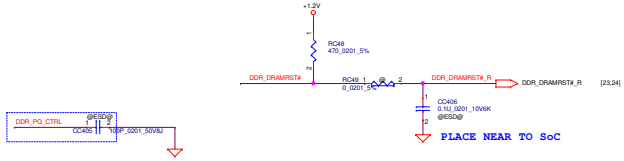
Date: Wednesday, March 02, 2022 Sheet 7 of 120

Follow Intel DDR4 NIL







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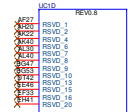

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			Date: Wednesday, March 02, 2022 Sheet 8 of 120

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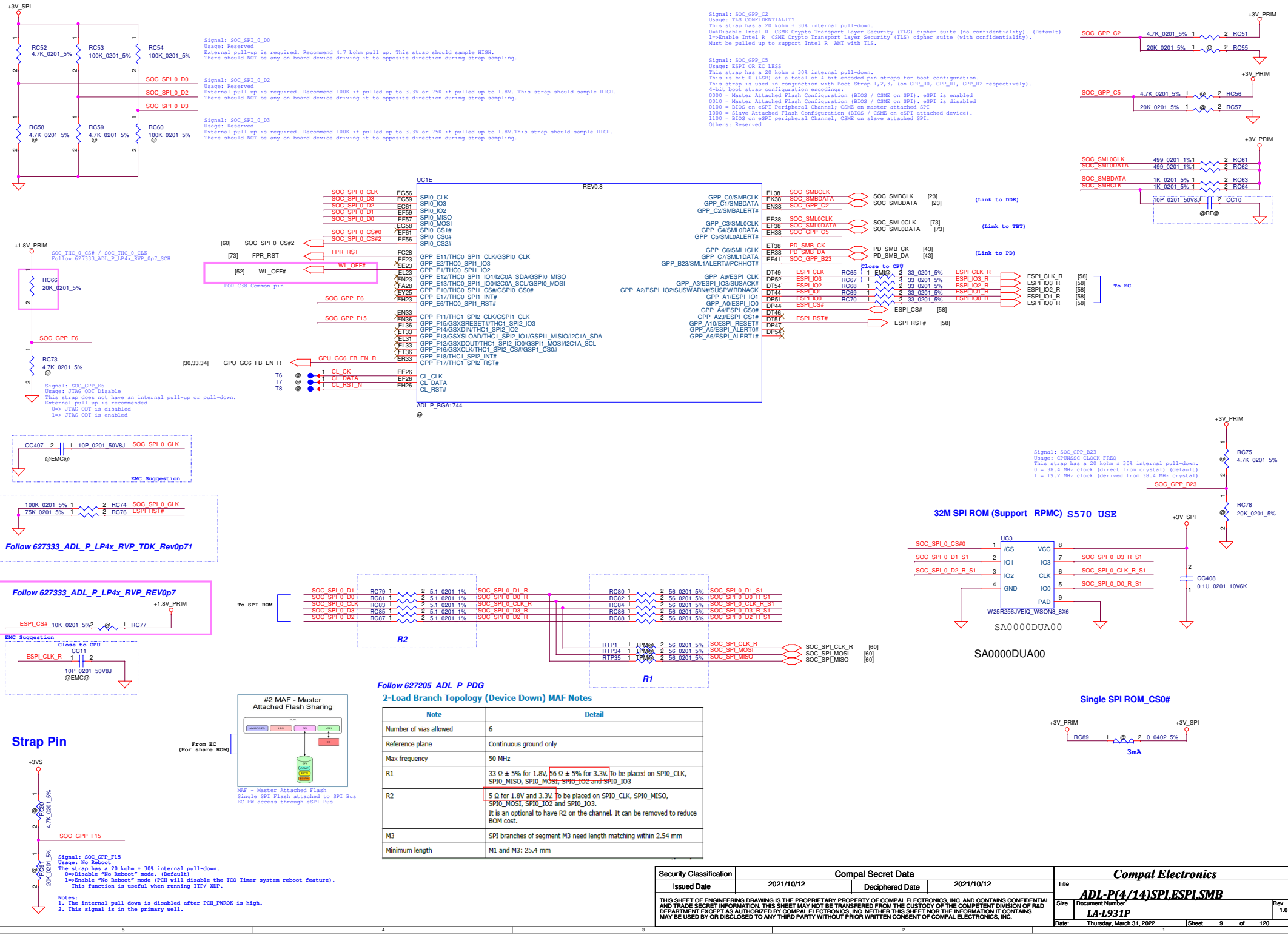

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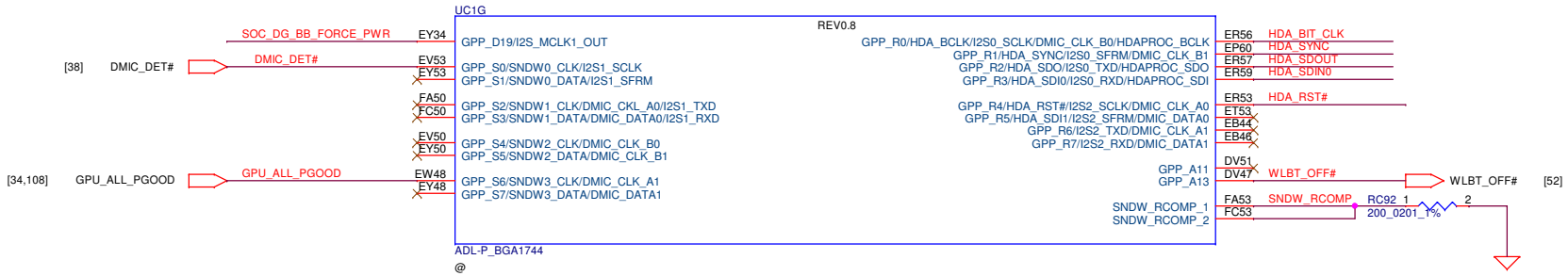
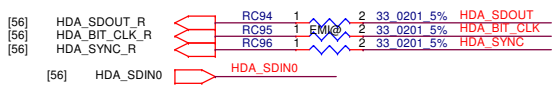
Size	Document Number	Rev
	LA-L931P	1.0

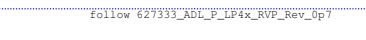
Date: Thursday, March 31, 2022 Sheet 9 of 120



HDA for AUDIO

RC96 Close to CPU





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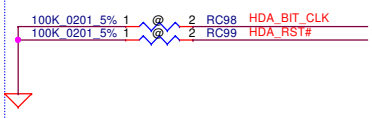
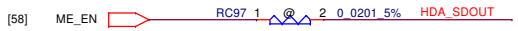


To Enable ME Override



Signal: HDA_SDOUT
Usage: FLASH DESCRIPTOR SECURITY OVERRIDE
This strap has a 20 kohm ± 30% internal pull-down.
0=>Enable security measures defined in the Flash Descriptor. (Default)
1=>Disable Flash Descriptor Security (override).
This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY.

Notes:
1. The internal pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

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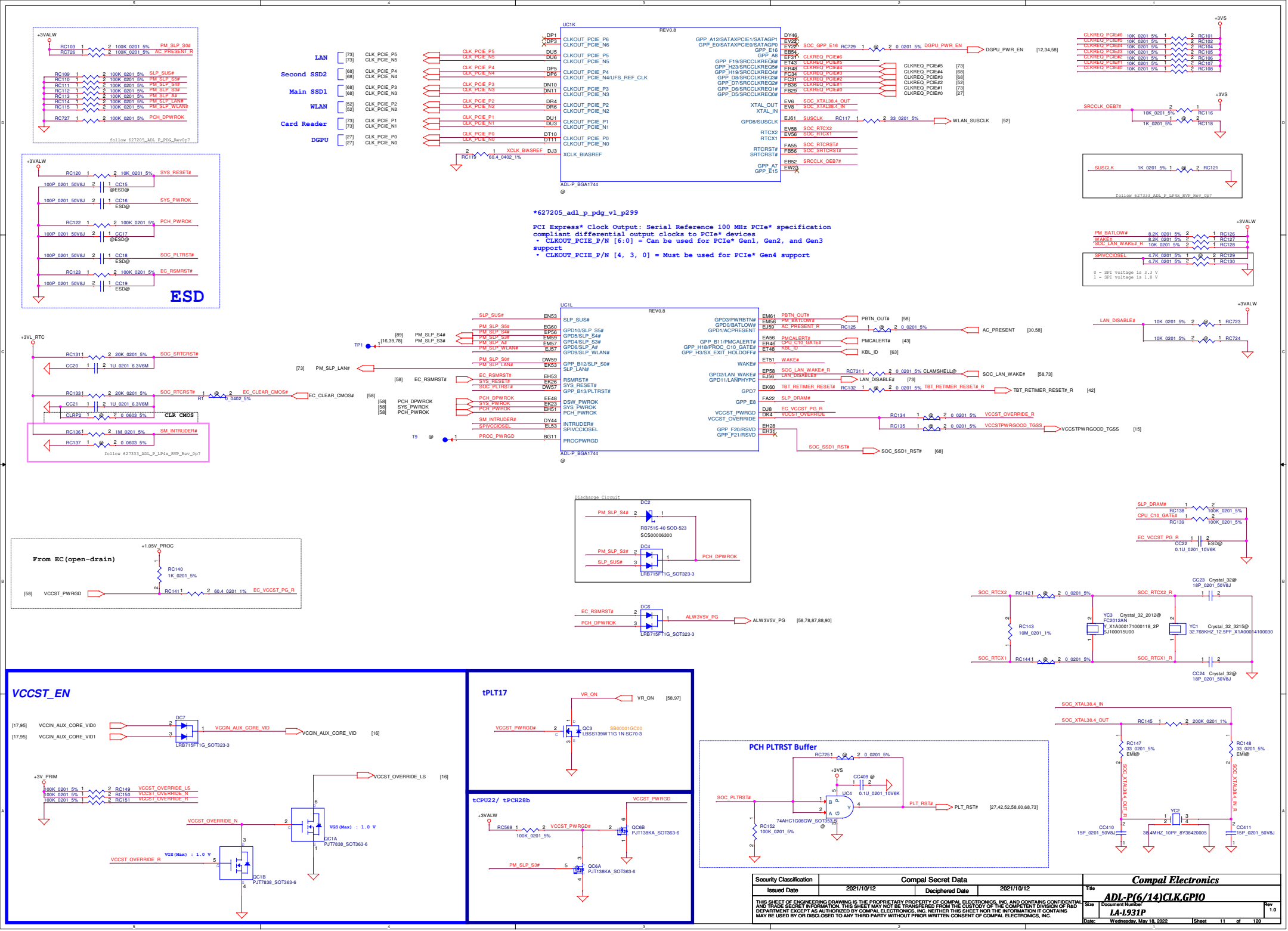
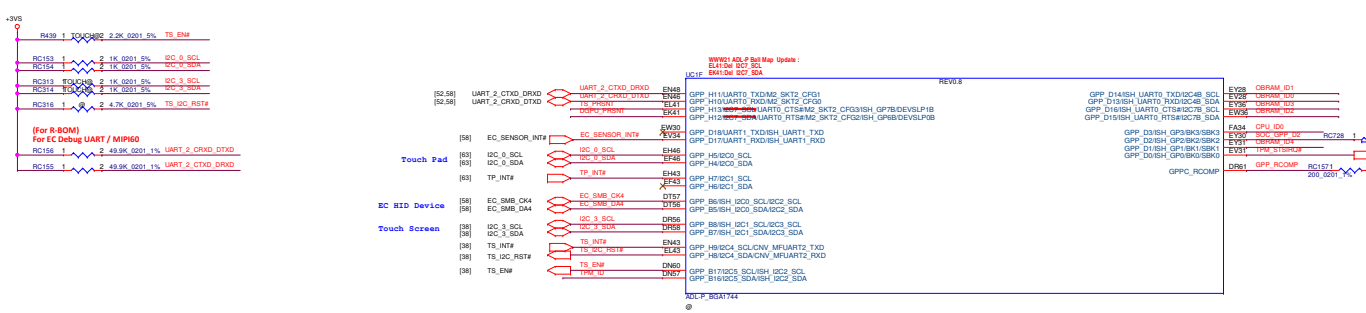
Title: ADL-P(5/14)HDA,SNDW

Size | Document Number: LA-L931P | Rev: 1.0

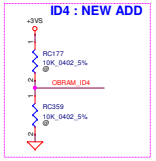
Date: Thursday, March 31, 2022 | Sheet 10 of 120

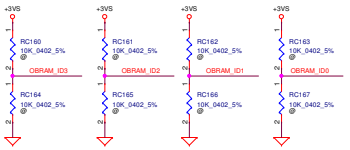

ESD
*627205_adl_p_pdg_v1_p299
PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices
• CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1, Gen2, and Gen3 support
• CLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support
From EC(open-drain)
VCCST_EN
tPLT17
tCPU22/ tPCH28b
PCH PLTRST Buffer
Compal Secret Data
Compal Electronics
ADL-P(6/14)CLK,GPIO
LA-L931P



On board RAM Straps

ID4 : NEW ADD



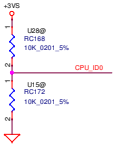


H: RC177 RC160 RC161 RC162 RC163

L: RC359 RC164 RC165 RC166 RC167

ADLP SDV	Capacity	Description	OBRAM ID4	OBRAM ID3	OBRAM ID2	OBRAM ID1	OBRAM ID0	BOM Structure	
		WITHOUT ON-BOARD RAM	L	L	L	L	L	NO MD@	SDP
	4GB	MICRON MT40A512M16TB-062E:J	L	L	L	L	H	DDR M4G@	SDP
		HYNIX H5AN8G6NCJR-XNC	L	L	L	H	L	DDR H4G@	SDP
V		SAMSUNG K4A8G165WC-BCWE	L	L	L	H	H	DDR S4G@	SDP
	8GB	MICRON MT40A1G16KD-062E:E	L	L	H	L	L	DDR M8G@	SDP
		HYNIX H5ANAG6NCMR-XNC	L	L	H	L	H	DDR H8G@	DDP
		Samsung K4AAG165WA-BCWE	L	L	H	H	L	DDR S8G@	SDP
V	4GB	MICRON MT40A512M16TB-062E:R	L	L	H	H	H	DDR M4GR@	SDP
V	8GB	Hynix H5ANAG6NCJR-XNC	L	H	L	L	L	DDR H8G SDP@	SDP
		MICRON MT40A1G16RC-062E:B	L	H	L	L	H	DDR M8G SDP@	SDP
		NA	L	H	L	H	L	@	
V	4GB	Hynix H5AN8G6NDJR-XNC	L	H	L	H	H	DDR H4G SDP@	SDP
V	8GB	Samsung K4AAG165WB-BCWE	L	H	H	L	L	DDR S8GA@	SDP
V	8GB	MICRON MT40A1G16TB-062E:F	L	H	H	L	H	DDR M8GA@	
		NA	L	H	H	H	L		
		NA	L	H	H	H	H		
		NA	H	L	L	L	L		
		RESERVED							

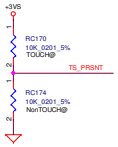
On board CPU Straps



Signal: CPU_ID0
LOW =CPU U15
HIGH=CPU U28

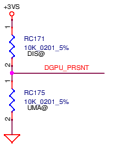
CPU_ID0	Status
U15	LOW
U28	High

Touch Screen Check Straps



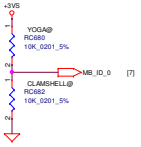
Signal: TS_PRSNT
0=Non-Touch Screen
1=Touch Screen

DIS & UMA Check Straps



Signal:DGPU_PRSNT
0=UMA
1=DIS

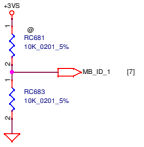
Project ID Straps



Signal: CPU_ID0
0=V350 ADL-P
1=V350 ADL-P YOGA

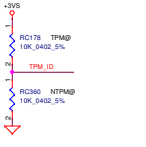
MB_ID_0	Status
ADL-P	LOW
ADL-P YOGA	High

Reserve for G-sensor



G-sensor_ID	Status
ST	0
BMA422	1

TPM STUFF



TPM_ID	Status
TPM Stuff	1
TPM un-Sutff	0

ON BOARD RAM

SDV (6)

UD1 DDR_S4G@ K4A8G165WC-BCWE SA0000CZ520	UD2 DDR_S4G@ K4A8G165WC-BCWE SA0000CZ520	UD3 DDR_S4G@ K4A8G165WC-BCWE SA0000CZ520	UD4 DDR_S4G@ K4A8G165WC-BCWE SA0000CZ520
UD1 DDR_H4G_SDP@ H5AN8G6NDJR-XNC SA0000CZ360	UD2 DDR_H4G_SDP@ H5AN8G6NDJR-XNC SA0000CZ360	UD3 DDR_H4G_SDP@ H5AN8G6NDJR-XNC SA0000CZ360	UD4 DDR_H4G_SDP@ H5AN8G6NDJR-XNC SA0000CZ360
UD1 DDR_M4GR@ MT40A512M16TB-062E:R SA0000CMS80	UD2 DDR_M4GR@ MT40A512M16TB-062E:R SA0000CMS80	UD3 DDR_M4GR@ MT40A512M16TB-062E:R SA0000CMS80	UD4 DDR_M4GR@ MT40A512M16TB-062E:R SA0000CMS80
UD1 DDR_H8G_SDP@ H5ANAG6NCJR-XNC SA0000DYB10	UD2 DDR_H8G_SDP@ H5ANAG6NCJR-XNC SA0000DYB10	UD3 DDR_H8G_SDP@ H5ANAG6NCJR-XNC SA0000DYB10	UD4 DDR_H8G_SDP@ H5ANAG6NCJR-XNC SA0000DYB10
UD1 DDR_S8GA@ K4AAG165WB-BCWE SA0000CZ280	UD2 DDR_S8GA@ K4AAG165WB-BCWE SA0000CZ280	UD3 DDR_S8GA@ K4AAG165WB-BCWE SA0000CZ280	UD4 DDR_S8GA@ K4AAG165WB-BCWE SA0000CZ280
UD1 DDR_M8GA@ MT40A1G16TB-062E:F SA0000F5320	UD2 DDR_M8GA@ MT40A1G16TB-062E:F SA0000F5320	UD3 DDR_M8GA@ MT40A1G16TB-062E:F SA0000F5320	UD4 DDR_M8GA@ MT40A1G16TB-062E:F SA0000F5320

RC359 DDR_S4G@ 10K_0402_5%	RC164 DDR_S4G@ 10K_0402_5%	RC165 DDR_S4G@ 10K_0402_5%	RC162 DDR_S4G@ 10K_0402_5%	RC163 DDR_S4G@ 10K_0402_5%
RC359 DDR_H4G_SDP@ 10K_0402_5%	RC160 DDR_H4G_SDP@ 10K_0402_5%	RC165 DDR_H4G_SDP@ 10K_0402_5%	RC162 DDR_H4G_SDP@ 10K_0402_5%	RC163 DDR_H4G_SDP@ 10K_0402_5%
RC359 DDR_M4GR@ 10K_0402_5%	RC164 DDR_M4GR@ 10K_0402_5%	RC161 DDR_M4GR@ 10K_0402_5%	RC162 DDR_M4GR@ 10K_0402_5%	RC163 DDR_M4GR@ 10K_0402_5%
RC359 DDR_H8G_SDP@ 10K_0402_5%	RC160 DDR_H8G_SDP@ 10K_0402_5%	RC165 DDR_H8G_SDP@ 10K_0402_5%	RC166 DDR_H8G_SDP@ 10K_0402_5%	RC167 DDR_H8G_SDP@ 10K_0402_5%
RC359 DDR_S8GA@ 10K_0402_5%	RC160 DDR_S8GA@ 10K_0402_5%	RC161 DDR_S8GA@ 10K_0402_5%	RC166 DDR_S8GA@ 10K_0402_5%	RC167 DDR_S8GA@ 10K_0402_5%
RC359 DDR_M8GA@ 10K_0402_5%	RC160 DDR_M8GA@ 10K_0402_5%	RC161 DDR_M8GA@ 10K_0402_5%	RC166 DDR_M8GA@ 10K_0402_5%	RC163 DDR_M8GA@ 10K_0402_5%

RC359 NO_MD@ 10K_0402_5%	RC164 NO_MD@ 10K_0402_5%	RC165 NO_MD@ 10K_0402_5%	RC166 NO_MD@ 10K_0402_5%	RC167 NO_MD@ 10K_0402_5%

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Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

Compal Electronics

Title: ADL-P(7/14)GPIO

Size: Document Number: LA-L931P Rev: 1.0

Date: Monday, March 28, 2022 Sheet 12 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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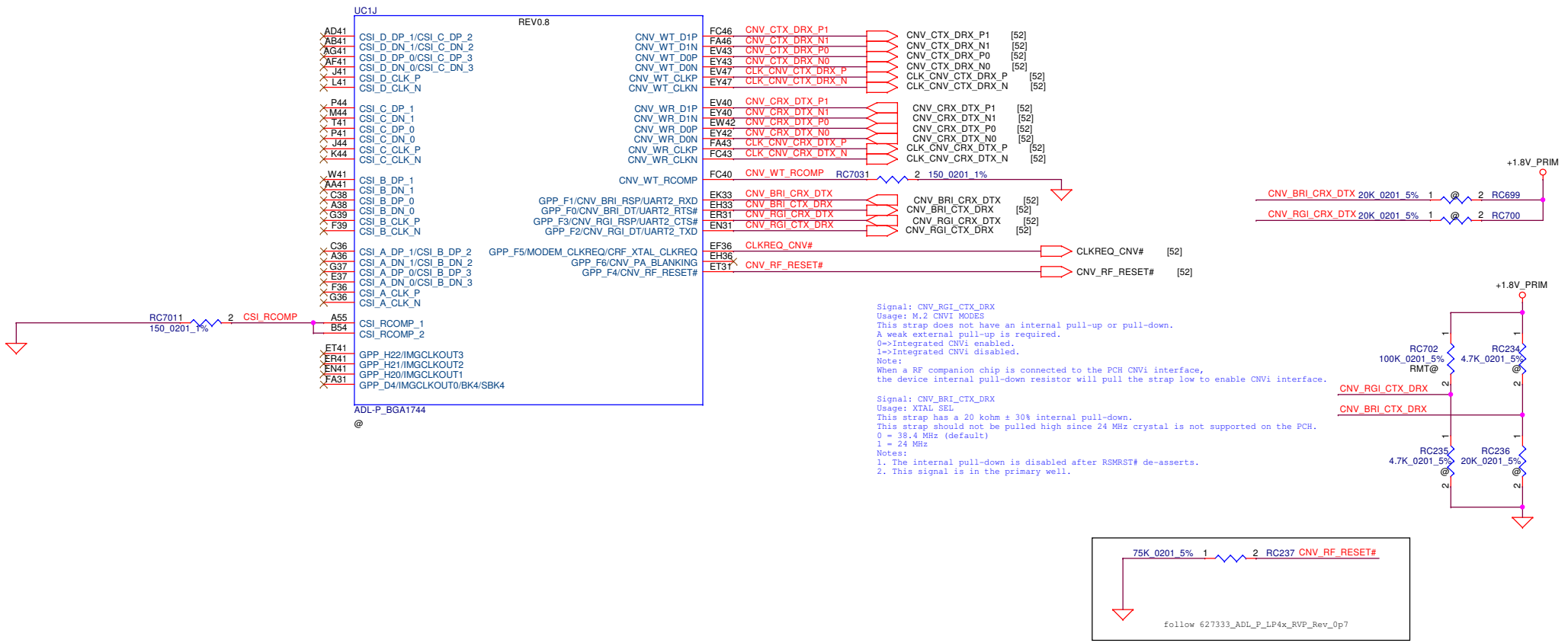
Compal Electronics			
Title	ADL-P(8/14)PCIE,USB,SATA		
Size	Document Number		Rev
	LA-L931P		1.0
Date:	Wednesday, March 02, 2022	Sheet 13 of 120	



Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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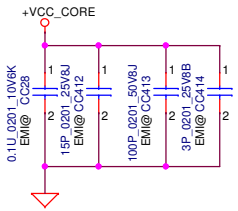
Compal Electronics

Title: ADL-P(9/14)CSI,CNVi

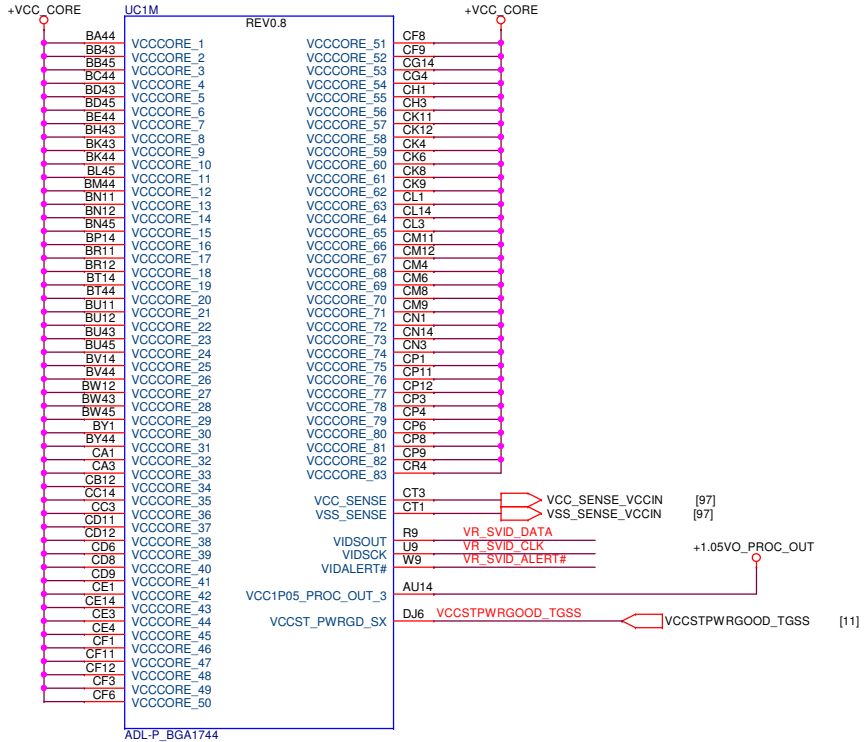
Size	Document Number	Rev
	LA-L931P	1.0

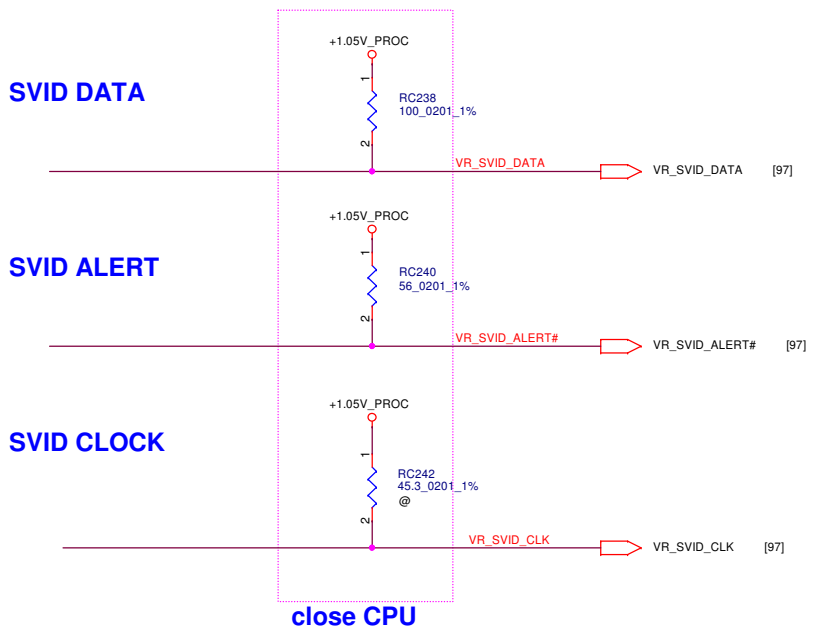
Date: Wednesday, March 02, 2022 Sheet 14 of 120

EMC CAPS-PLACE
< 5mm from SOC VCCIN
0.1uF *1
100pF *1
15pF *1
3pF *1



626549_ADL_P_BEP_plus_TDK_Rev0p71





Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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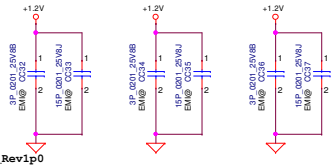
Compal Electronics

Title: ADL-P(10/14)Power, SVID

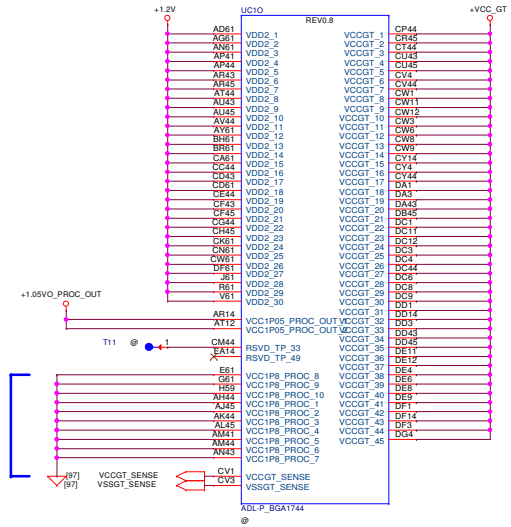
Size | Document Number: LA-L931P | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 15 of 120

EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
15pF* 3 (EMI@)
3pF* 3 (EMI@)

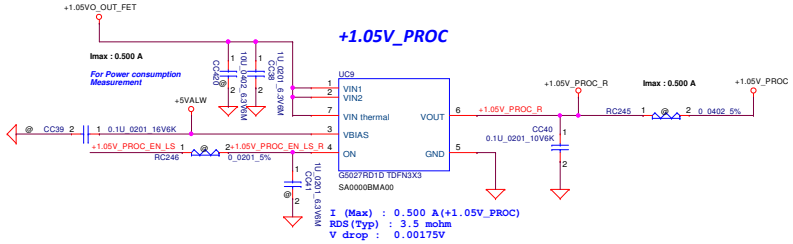


631621_ADL_P_DDR5_SODIMM_1DPC_T3_RVP_TDK_Rev1p0

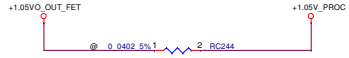


When using PCIe PEG10 configured to Gen5 or lower, it is recommended to use an LDO solution for this rail. If disabling the PCIE port, these pins can be connected to GND. Processor PCIe 010 can be disabled through the use of FIT tool. For further details and instructs, please follow the FIT programmers guide.

+1.05V_PROC



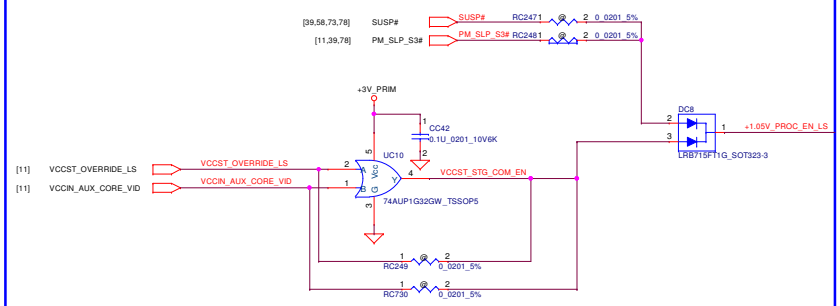
627205_ADL_P_PDG_Rev1.0



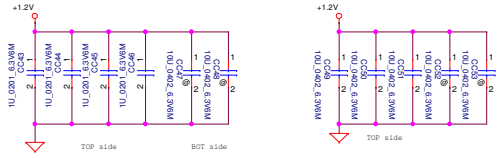
NOTE

Sideband signals(PECI,THERMTRIP,PROCHOT,VCCST_PWRGD,SVID) should be connected to **VCC1P05_PROC** rail when there is Power Gate or to **VCC1P05_OUT_FET** (which should be shorted to VCC1P05_OUT_FET)rail when there is no Power Gate.

+1.05V_PROC Enable



1uF* 6
10uF * 3
uF * 2
Follow 627205_ADL P_PDG_Rev1P0



Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics			
Title: ADL-P(11/14)Power			
Size	Document Number: LA-L931P		Rev: 1.0
Date: Thursday, March 31, 2022	Sheet 16 of 120		

+1.8VALW TO +1.8V_PRIM

+1.8VALW — RC2531 @ 2 0_0603_5% — +1.8V_PRIM
I Max = 1.3A
CC54 4.7U_0402_6.3V6M

+3VALW — RC250 1 @ 2 0_0402_5% — +3VALW_DSW
+3V_PRIM — RC251 1 @ 2 0_0402_5% — +3V_PRIM_SOC
I Max = 0.202A

+1.8V_PRIM_MCP — @L1 1 2 0.68UH_UHP252012NF-R68M_3A_20%-X — +1.8V_VCCA_CLKLDO
0_0402_5% 1 @ 2 RC254
RC255 0_0402_5%
2 1 CC55 22U_0603_6.3V6M
2 1 CC56 22U_0603_6.3V6M

+1.8V_PRIM — RC2521 @ 2 0_0603_5% — +1.8V_PRIM_MCP
I Max = 0.17A

+3V_PRIM — RC256 1 @ 2 0_0402_5% — +3V_VCCPGPPR

NOTE:
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO

VCC_MIPILP

If the platform uses MIPI-DSI connect a LDO to the VCC_MIPILP pin, leave the VCC_DISPIO and VCC1P05_OUT floating.

If the platform does not use MIPI-DSI, leave the VCC_MIPILP pin floating and short VCC_DISPIO and VCC1P05_OUT.

UC1N — REV0.8 — ADL-P_BGA1744

+VCCIN_AUX
AL20 VCCIN_AUX_1
AL32 VCCIN_AUX_2
AN20 VCCIN_AUX_3
AN22 VCCIN_AUX_4
AN30 VCCIN_AUX_5
AN32 VCCIN_AUX_6
AN37 VCCIN_AUX_7
AP17 VCCIN_AUX_8
AP27 VCCIN_AUX_9
AP30 VCCIN_AUX_10
AP32 VCCIN_AUX_11
AP37 VCCIN_AUX_12
B3 VCCIN_AUX_13
D3 VCCIN_AUX_14
E1 VCCIN_AUX_33
F1 VCCIN_AUX_36
F3 VCCIN_AUX_37
G3 VCCIN_AUX_38
H4 VCCIN_AUX_39
J1 VCCIN_AUX_40
J3 VCCIN_AUX_41
L1 VCCIN_AUX_42
L3 VCCIN_AUX_43
N3 VCCIN_AUX_44
DH45 VCCIN_AUX_15
DJ41 VCCIN_AUX_16
DJ44 VCCIN_AUX_17
DK40 VCCIN_AUX_18
DK43 VCCIN_AUX_19
DK45 VCCIN_AUX_20
DL44 VCCIN_AUX_21
DM1 VCCIN_AUX_22
DM14 VCCIN_AUX_23
DM43 VCCIN_AUX_24
DP41 VCCIN_AUX_25
DP42 VCCIN_AUX_26
DR14 VCCIN_AUX_27
DR40 VCCIN_AUX_28
DT41 VCCIN_AUX_29
DU14 VCCIN_AUX_30
DU40 VCCIN_AUX_31
DV2 VCCIN_AUX_32
ED2 VCCIN_AUX_34
EL2 VCCIN_AUX_35
P1 VCCIN_AUX_FLTR

+VCCIN_AUX_FIL — TOP side — CC58 2 22U_0603_6.3V6M — CC59 2 22U_0603_6.3V6M — C220 1 2 10U_0402_6.3V6M

+1.05VO_EXTBYPASS — RC258 100K_0201_5% — +1.05VO_VNNBYPASS — RC259 100K_0201_5%

[95] VSS_SENSE_AUX
[95] VCC_SENSE_AUX
AH30 VSSINAUX_SENSE
AF30 VCCINAUX_SENSE

EF21 VCC_VNNEXT_1P05_1
EH21 VCC_VNNEXT_1P05_2

EE18 VCC_V1P05EXT_1P05_1
EE21 VCC_V1P05EXT_1P05_2

[7] VCCIN_AUX_CORE_ALERT#_R — RC2601 @ 2 0_0201_5% — VCCIN_AUX_CORE_ALERT#
DT59 GPP_B2/VRALERT#
VNN_CTRL — T16 @ — EK31 GPP_F22/VNN_CTRL
V1.05P_CTRL — T17 @ — EL28 GPP_F23/V1P05_CTRL

[11,95] VCCIN_AUX_CORE_VID0
[11,95] VCCIN_AUX_CORE_VID1
VCCIN_AUX_CORE_VID0 — EA60 GPP_B0/CORE_VID0
VCCIN_AUX_CORE_VID1 — EA58 GPP_B1/CORE_VID1

+1.8V_PRIM_MCP
DW20 VCCPRIM_1P8_1
DW22 VCCPRIM_1P8_2
DW27 VCCPRIM_1P8_3
DW30 VCCPRIM_1P8_4
DY21 VCCPRIM_1P8_5
DY23 VCCPRIM_1P8_6
DY26 VCCPRIM_1P8_7
DY28 VCCPRIM_1P8_8
DY31 VCCPRIM_1P8_9
EB18 VCCPRIM_1P8_12
EB21 VCCPRIM_1P8_13
EB23 VCCPRIM_1P8_14
EB28 VCCPRIM_1P8_15
EC14 VCCPRIM_1P8_16
EC16 VCCPRIM_1P8_17
EC23 VCCPRIM_1P8_18
EC26 VCCPRIM_1P8_19
EE14 VCCPRIM_1P8_20
EE28 VCCPRIM_1P8_21
EG14 VCCPRIM_1P8_22
FB33 VCCPRIM_1P8_23

+3V_PRIM_SOC
DV41 VCCPRIM_3P3_1
DW40 VCCPRIM_3P3_2
EB33 VCCPRIM_3P3_3
EC31 VCCPRIM_3P3_5
EC33 VCCPRIM_3P3_6
EE31 VCCPRIM_3P3_7

FB45 RSVD_24
+0.85VO_VCCLDOSTD — FB52 VCCLDOSTD_0P85
+1.8V_VCCA_CLKLDO — EJ14 VCCA_CLKLDO_1P8_1 — EM14 VCCA_CLKLDO_1P8_2
+1.24VO_VCCDPHY — FB39 VCCDPHY_1P24

BN43 RSVD_TP_28
AY11 RSVD_TP_18 — 1 @ T12
BP44 RSVD_TP_29
BL12 RSVD_TP_27 — 1 @ T13
CN43 RSVD_TP_34 — 1 @ T14
BJ11 RSVD_TP_24

+1.05VO_OUT_PCH
EB36 VCCPRIM1P05_OUT_PCH_1
EC36 VCCPRIM1P05_OUT_PCH_3
+1.05VO_VCCDSW — EE41 VCCDSW_1P05
+1.24V_MIPI — V1 — 1 @ T15 — EB38 VCC_MIPILP
EE36 VCCPRIM1P05_OUT_PCH_2
VCCPRIM1P05_OUT_PCH_4

+1.05VO_OUT_PCH
+3VL_RTC — EC38 VCCRTC
+3VALW_DSW — EB42 VCCPDSW_3P3
+3V_VCCPGPPR — EE33 VCCPGPPR

+3V_PRIM_SOC — EB41 VCCPRIM_3P3_4
+1.8V_PRIM_MCP — DY41 VCCPRIM_1P8_10
DY42 VCCPRIM_1P8_11

+1.05V_PROC — EU1 VCC1P05_PROC_1 — EU4 VCC1P05_PROC_2

+1.05VO_OUT_FET — EV3 VCC1P05_OUT_FET_1 — EW1 VCC1P05_OUT_FET_2 — EY1 VCC1P05_OUT_FET_3

+1.05VO_PROC_OUT — AM15 VCC_DISPIO

BJ12 RSVD_TP_25
BK14 RSVD_TP_26
BF14 RSVD_TP_21

@

+3VALW TO +3V_PRIM

+3VALW — RC257 1 @ 2 0_0402_5% — +3V_PRIM
C207 0.1U_0201_10V6K @
UC12 @ SY6288C20AAC_SOT23-5: IN, OUT, GND, EN, OC
[58,90] 3VP_1.8VA_EN — 3VP_1.8VA_EN
CC57 4.7U_0402_6.3V6M

+3V_PRIM_SOC — CC60 1U_0201_6.3V6M — CC61 0.1U_0201_10V6K
+0.85VO_VCCLDOSTD — CC62 22U_0402_6.3V6M
+1.05VO_VCCDSW — CC63 1U_0201_6.3V6M
+1.24VO_VCCDPHY — CC64 4.7U_0402_6.3V6M
+1.05V_PROC — CC65 1U_0201_6.3V6M — CC66 1U_0201_6.3V6M
+3VALW_DSW — CC67 1U_0201_6.3V6M

PLACE CAP CLOSEST POSSIBLE TO THE BGA

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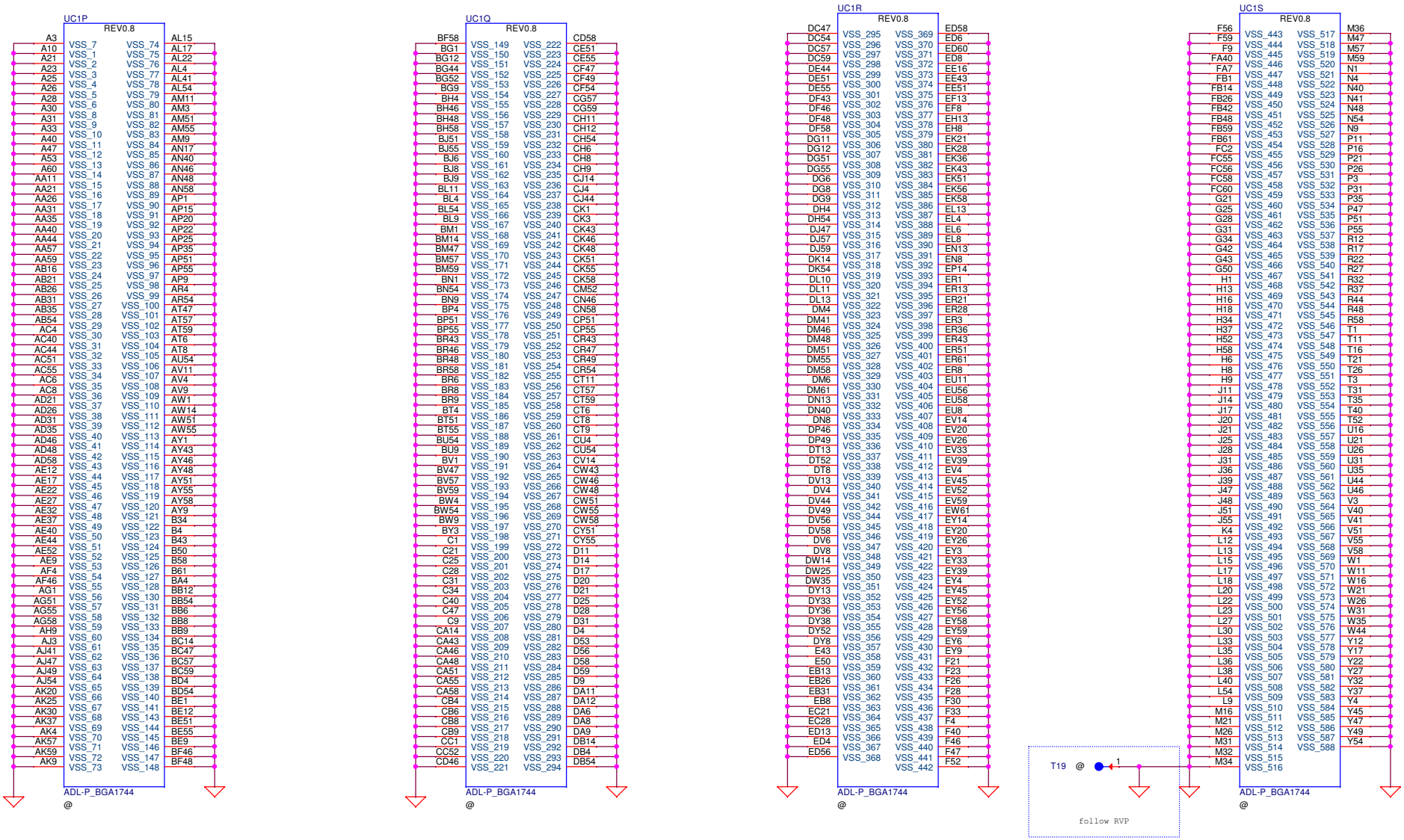
Compal Electronics

Title: ADL-P(12/14)Power

Size: — Document Number: LA-L931P — Rev: 1.0

Date: Thursday, March 31, 2022 — Sheet 17 of 120



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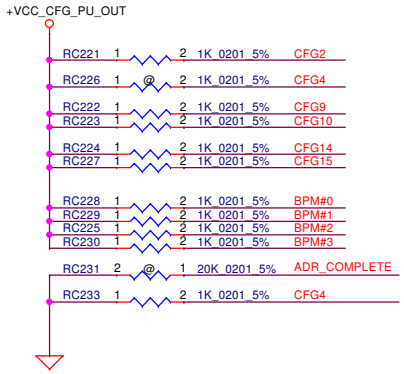
Compal Electronics

Title: **ADL-P(13/14)GND**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Wednesday, March 02, 2022 | Sheet 18 of 120



CFG Signals Functionality and Termination

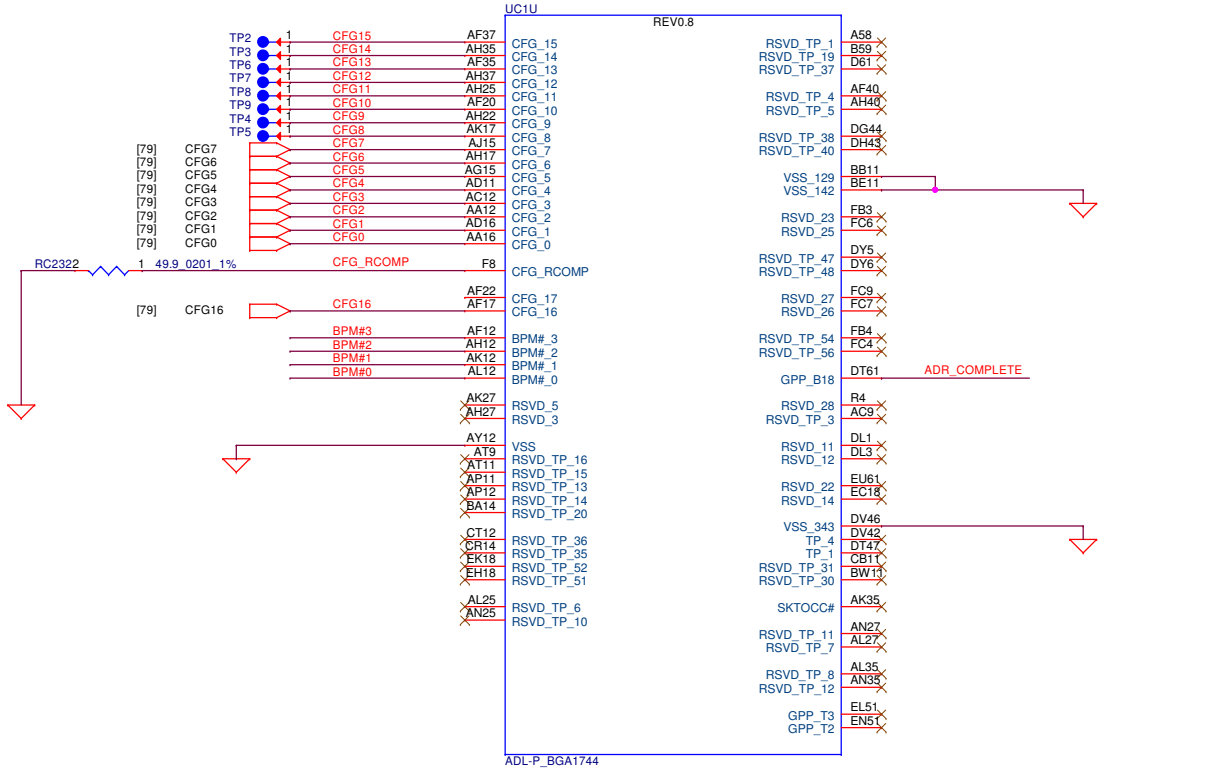
CFG Signals Functionality and Termination

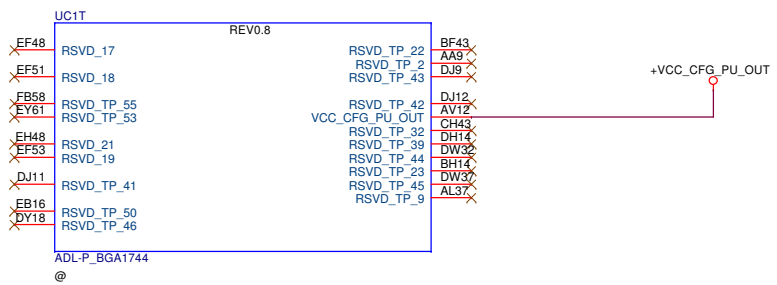
CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	none	
CFG[2]	PCI Express* Static X8 Lane Numbering Reversal • 1:Normal Operation • 0: Lane Numbers reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[3]	RSVD	None	
CFG[4]	RSVD	None	
CFG[5]	RSVD	None	
CFG[6:7]	RSVD	None	
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	None	
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull-up to VCC_CFG_PU_OUT/ / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

ADL P CFG15 was erroneously stated as reserved and CFG14 was marked as shared pin for lane reversal for PEG60 and PEG62

Below is the updated 'CFG Signal Functionality and Termination' table for ADL P (PDG Section – 5.7, Table 359)

CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[15]	PEG62 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm





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Title: ADL-P(14/14)RSVD,CFG

Size | Document Number: LA-L931P | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 19 of 120

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			Document Number: LA-L931P	Rev: 1A
			Date: Tuesday, January 04, 2022	Sheet 30 of 100

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Title: **Reserve for SOC/PCH/FCH EE**

Size	Document Number	Rev
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Date: Tuesday, January 25, 2022 | Sheet 21 of 120

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

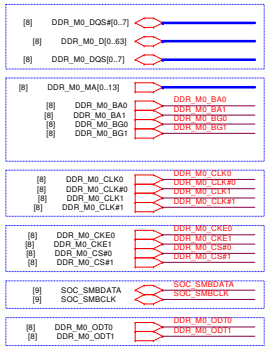
Title: **Reserve for SOC/PCH/FCH EE**

Size	Document Number	Rev
	LA-L931P	1.0

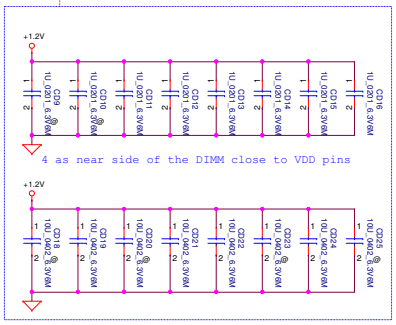
Date: Tuesday, January 25, 2022 | Sheet 22 of 120

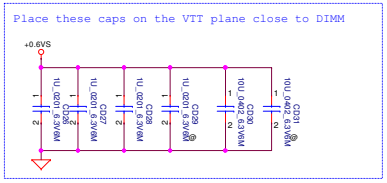
Standard Type

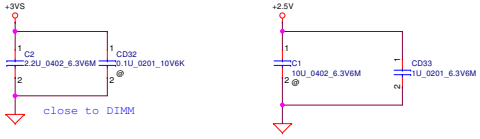
2-3A to 1 DIMMs/channel

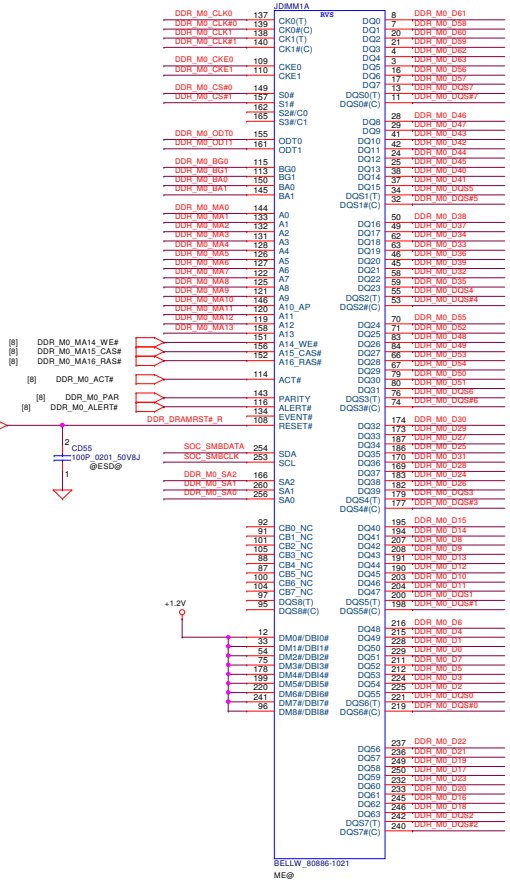


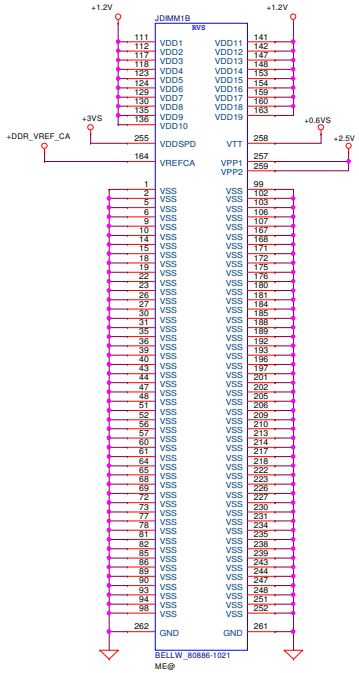
Layout Note:
Place near JDIMM1

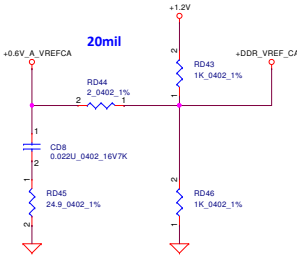






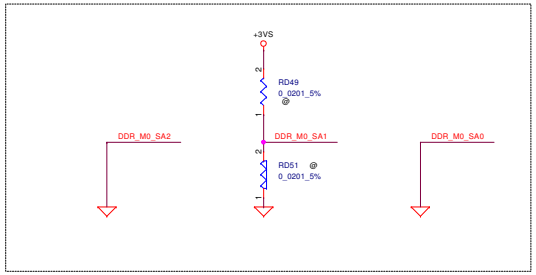






Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

JDIMM1 ADDRESS PLACE CLOSE TO DIMM)



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			Size: Document Number: LA-L931P Rev: 1.0
			Date: Thursday, March 31, 2022 Sheet 23 of 120

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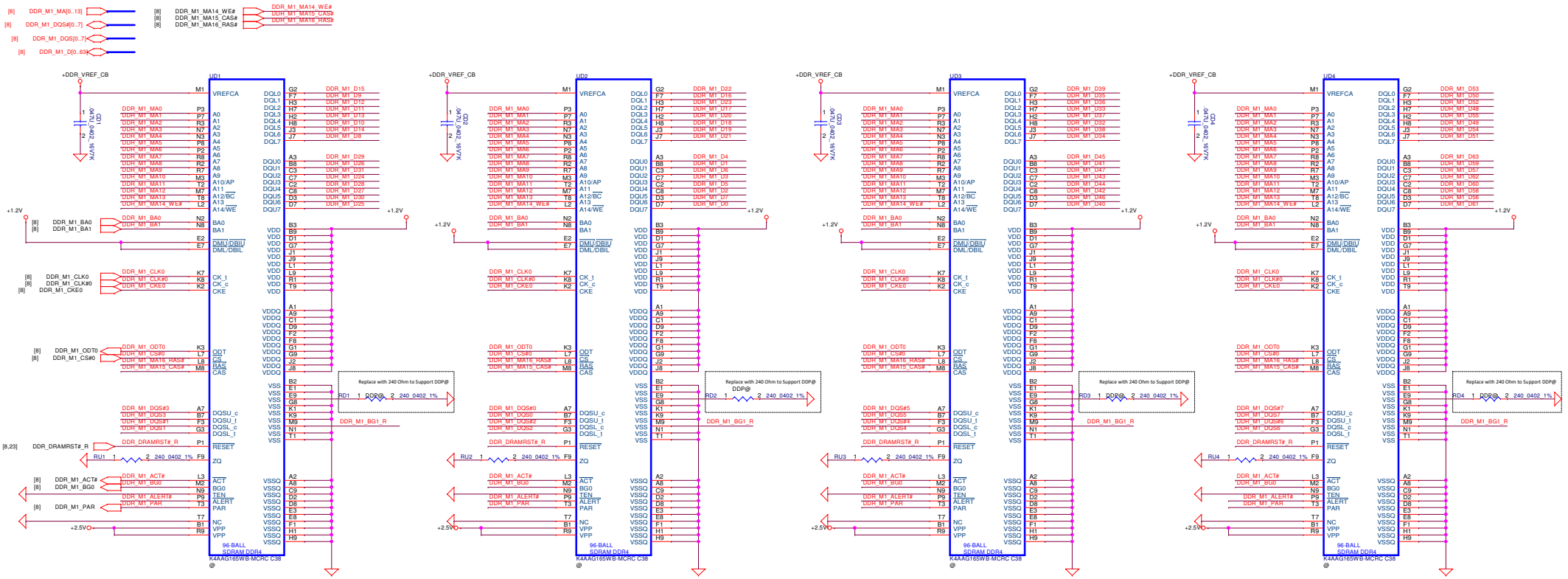
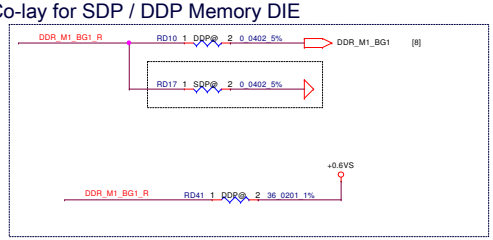
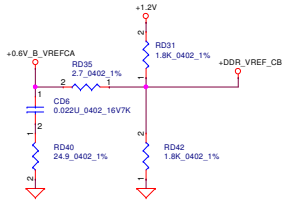
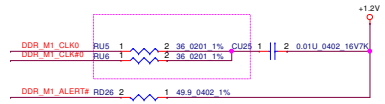


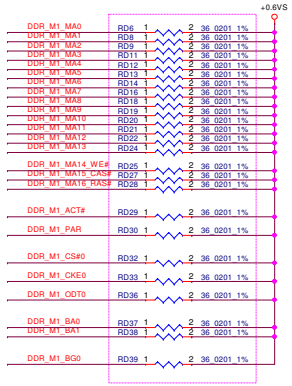
Co-lay for SDP / DDP Memory DIE

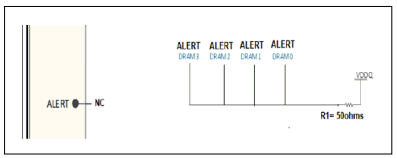




CLOCK TERMINATION







627205 ADLP PDG REV1.2

Note	Detail
Vref	Same Vref recommendation as SKL
ALERT pin	ALERT pin is not used and can be left unconnected, pull-up required on DRAM. Refer topology diagram.
Serpentine routing	Use 3x of dielectric height for serpentine routing spacing
Rtt/Ctt for CLK	R1=36ohm; C2=0.01uF
Rtt for CMD/CTRL	Rtt=36ohm
Rtt/Ctt for RESET	R1=470ohm 5%; R2=0ohm; C1=0.1uF (no stuff)
Rtt/Ctt for Vref	Refer to Fig.
RCOMP value	100ohm

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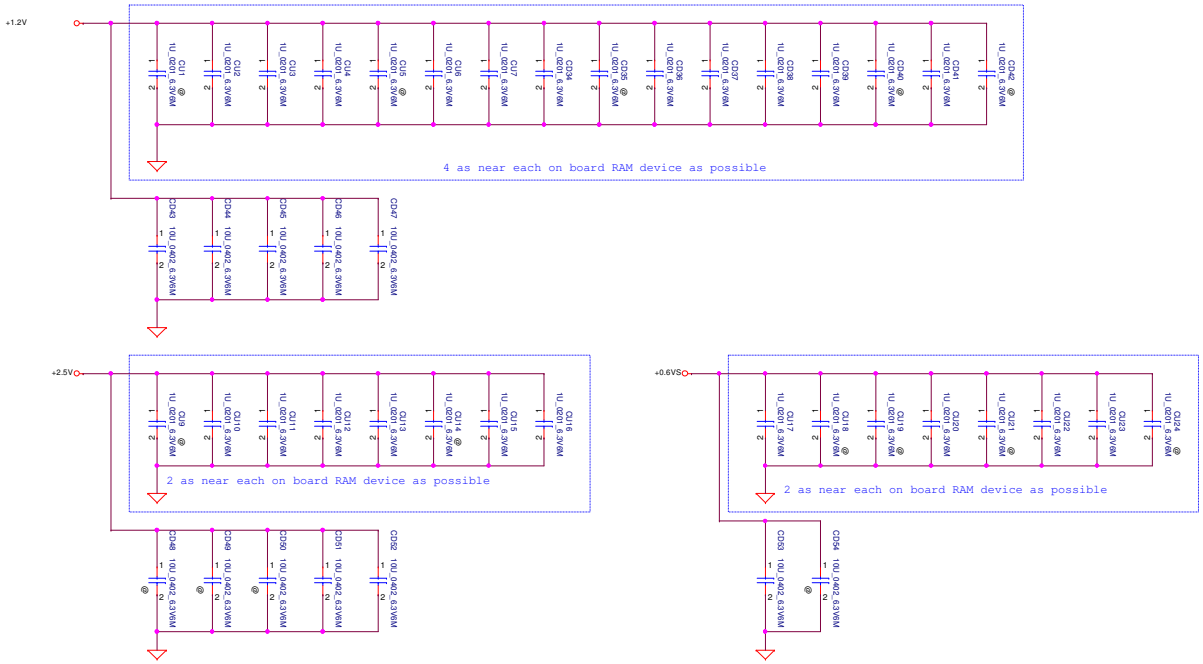
Title: DDR4 CHM0: DIMM0 EE

Size: | Document Number: LA-1931P | Rev: 1.0

Date: Monday, March 28, 2022 | Sheet 24 of 120



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Title: **DDR4_CHM1: DIMM1_EE**

Size	Document Number	Rev
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Title: **Reserve for DDR3_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 26 of 120

GPU

GN18_chip@
UV1
SA0000EG550
GN18-S5

GN20_Chip@
UV1
SA0000EJE50
GN20-S5

UV1A
NV
COMMON

1/14 PCI_EXPRESS

PCIE CLK

[11] CLK_PCIE_P0
[11] CLK_PCIE_N0

PCIE X4 Bus

[13] PCIE_CRX_DTX_P5
[13] PCIE_CRX_DTX_N5
[13] PCIE_CTX_DRX_P5
[13] PCIE_CTX_DRX_N5
[13] PCIE_CRX_DTX_P6
[13] PCIE_CRX_DTX_N6
[13] PCIE_CTX_DRX_P6
[13] PCIE_CTX_DRX_N6
[13] PCIE_CRX_DTX_P7
[13] PCIE_CRX_DTX_N7
[13] PCIE_CTX_DRX_P7
[13] PCIE_CTX_DRX_N7
[13] PCIE_CRX_DTX_P8
[13] PCIE_CRX_DTX_N8
[13] PCIE_CTX_DRX_P8
[13] PCIE_CTX_DRX_N8

[30] PLT_RST_VGA#

					AG30	PEX_WAKE#
PLT_RST_VGA#					AG29	PEX_RST#
CLKREQ_PEG#0_R					AG31	PEX_CLKREQ#
CLK_PCIE_P0					AE30	PEX_REFCLK
CLK_PCIE_N0					AE31	PEX_REFCLK#
PCIE_CRX_DTX_P5	CV8	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_P5	AC27 PEX_TX0
PCIE_CRX_DTX_N5	CV9	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_N5	AC28 PEX_TX0#
PCIE_CTX_DRX_P5	CV1	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_P5	AC30 PEX_RX0
PCIE_CTX_DRX_N5	CV10	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_N5	AC31 PEX_RX0#
PCIE_CRX_DTX_P6	CV11	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_P6	AA27 PEX_TX1
PCIE_CRX_DTX_N6	CV12	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_N6	AA28 PEX_TX1#
PCIE_CTX_DRX_P6	CV13	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_P6	AA31 PEX_RX1
PCIE_CTX_DRX_N6	CV15	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_N6	AA30 PEX_RX1#
PCIE_CRX_DTX_P7	CV17	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_P7	W27 PEX_TX2
PCIE_CRX_DTX_N7	CV18	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_N7	W28 PEX_TX2#
PCIE_CTX_DRX_P7	CV19	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_P7	W31 PEX_RX2
PCIE_CTX_DRX_N7	CV20	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_N7	W30 PEX_RX2#
PCIE_CRX_DTX_P8	CV21	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_P8	U28 PEX_TX3
PCIE_CRX_DTX_N8	CV22	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CRX_C_DTX_N8	U27 PEX_TX3#
PCIE_CTX_DRX_P8	CV23	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_P8	U30 PEX_RX3
PCIE_CTX_DRX_N8	CV24	DIS@	1 2	0.22U_0201_6.3V6M	PCIE_CTX_C_DRX_N8	U31 PEX_RX3#

Near UV1

Reset Control

(From PCH)
[11,42,52,58,60,68,73] PLT_RST#
[7] DGPU_HOLD_RST#
(From GPU)

+1.8VGS_AON
UV2 DIS@
NL17SZ08EDFT2G_SOT353-5
SA0000BJI00
IN B, VCC, OUT Y, IN A, GND
PLT_RST#
DGPU_HOLD_RST#
PLT_RST_VGA#
RV1 100K_0201_5% DIS@

CLK_REQ

+1.8VGS_AON
+1.8VGS_AON
RV2 10K_0201_5% DIS@
QV1 DIS@ BSS138W-7-F_SOT323-3
CLKREQ_PEG#0_R
(To SOC)
CLKREQ_PCIE#0 [11]
VGS(Max) : 1.5 V
RV4 10K_0201_5% @
RV6 0_0402_5%

(GN20=0.95V、GN18=1V) (1.713A)
+1.0VS_DGPU
PEX_DVDD:1uf*4、10uf*2
PEX_CVDD:4.7uf*1、22uf*1
Place near balls
Place between GPU and VR

PEX_DVDD AA25, U25, V25, V26, W25, Y25, Y26
CV2 1U_0201_6.3V6M DIS@
CV3 1U_0201_6.3V6M DIS@
CV4 1U_0201_6.3V6M DIS@
CV5 1U_0201_6.3V6M DIS@
CV6 10U_0402_6.3V6M DIS@
CV7 10U_0402_6.3V6M DIS@

Place near balls
Place between GPU &VR
CV14 4.7U_0402_6.3V6M DIS@
CV16 220U_6032_6.3V6M DIS@
PEX_HVDD:1uf*3、10uf*2

(1.8V) (1.640A)
+1.8VGS_AON
PEX_CVDD AB25, AB26

Place near balls
Place between GPU and VR
PEX_HVDD AC25, AD25, AE26, AE27, AE28
CV25 1U_0201_6.3V6M DIS@
CV26 1U_0201_6.3V6M DIS@
CV27 1U_0201_6.3V6M DIS@
CV28 10U_0402_6.3V6M DIS@
CV29 10U_0402_6.3V6M DIS@

PEX_PLL_HVDD AD26

(1.8V) (0.40A)
+1.8VGS_AON
PEX_PLL_HVDD:4.7uf*1、22uf*1
Place near balls
Place between GPU and VR
CV30 4.7U_0402_6.3V6M DIS@
CV31 220U_6032_6.3V6M DIS@

PEX_CVDD_SENSE R30
PEX_TERMP R31 PEX_TERMP
RV7 2.49K_0402_1% DIS@

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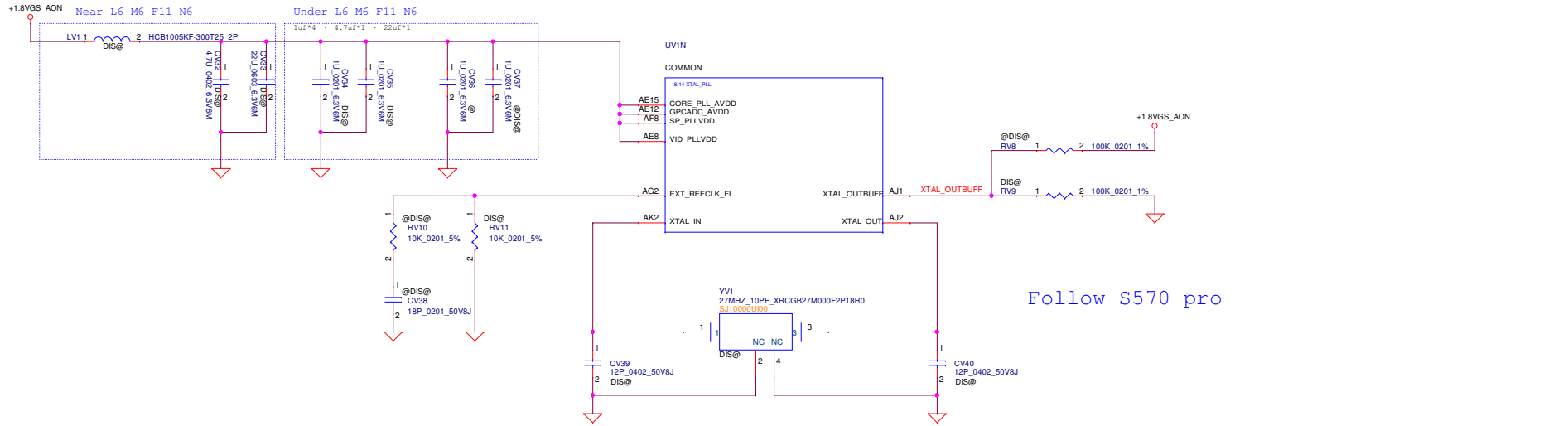
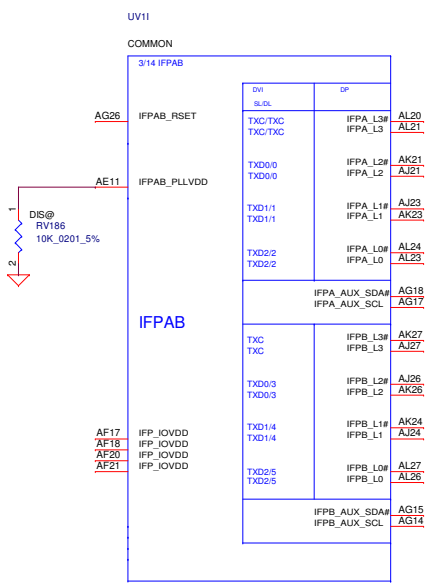
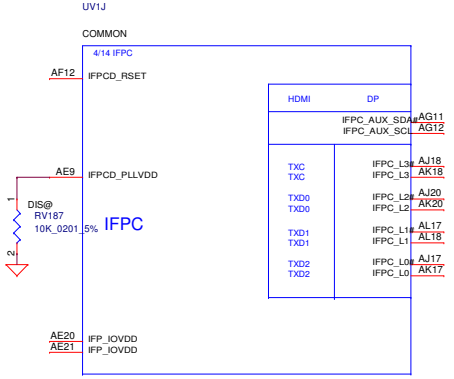
Size	Document Number	Rev
	LA-L931P	1.0

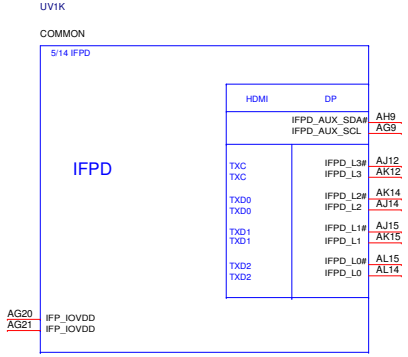
Date: Wednesday, August 31, 2022 Sheet 27 of 120

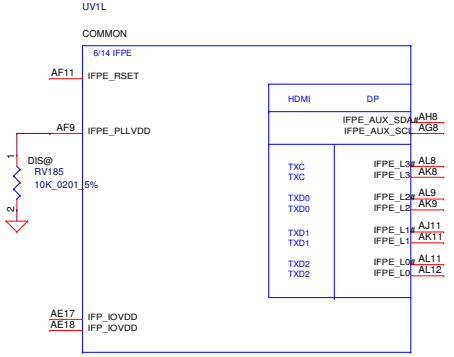
X'TAL











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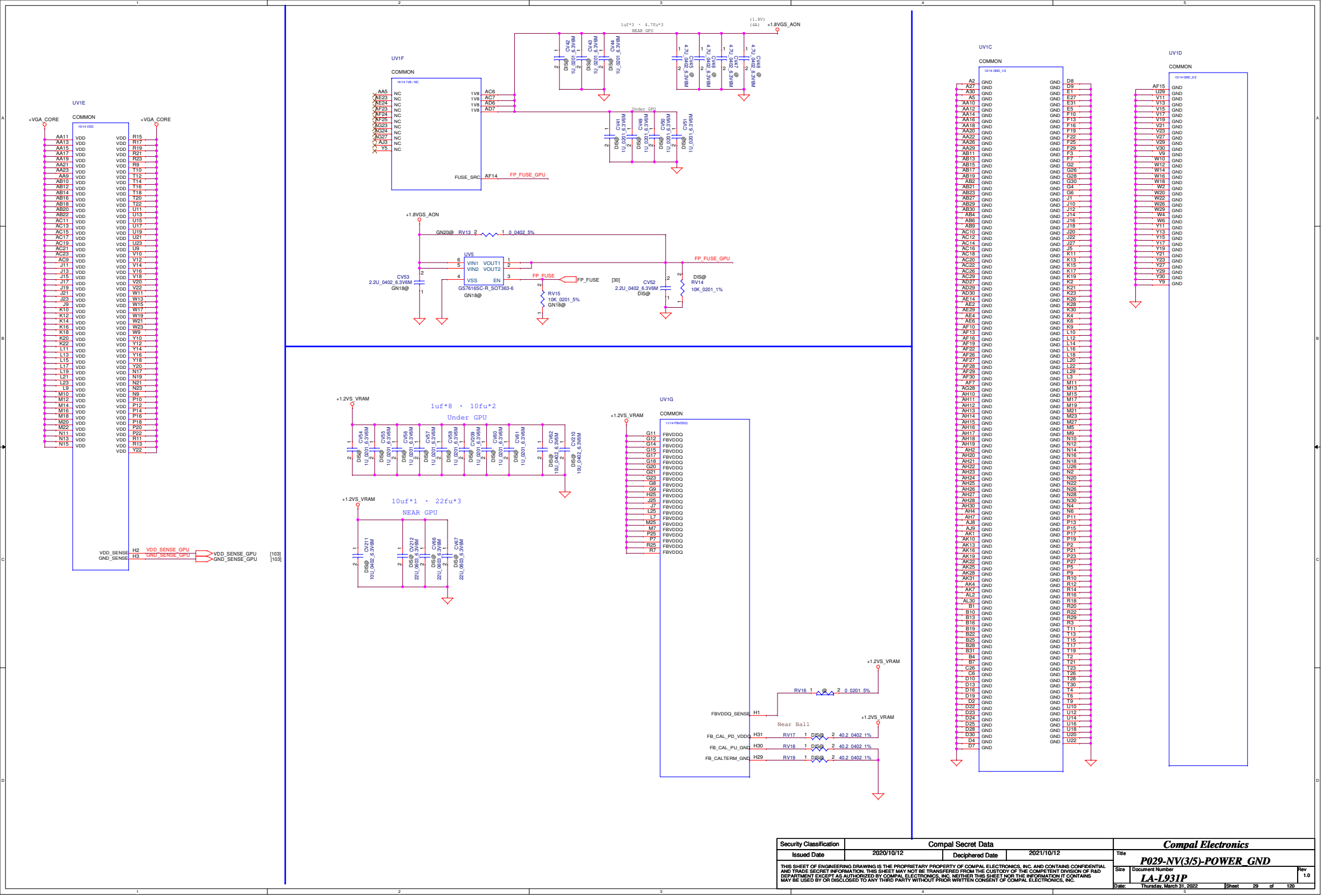
Compal Electronics	
Title	P028-NV(2/5)-IFP_XTAL
Size	Document Number: LA-L931P
Rev	1.0
Date:	Monday, March 28, 2022
Sheet	28 of 120



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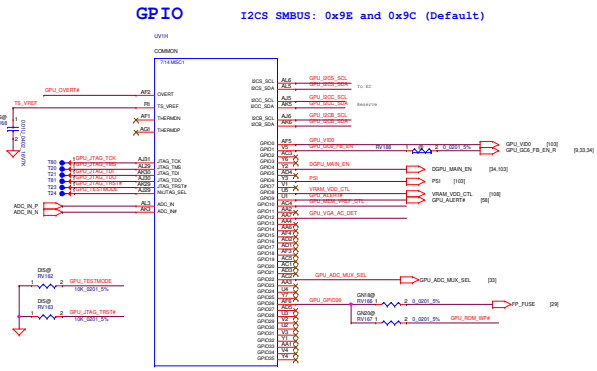
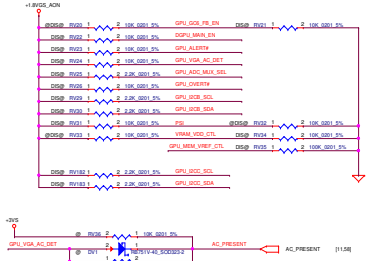
Size	Document Number	Rev
	LA-L931P	1.0

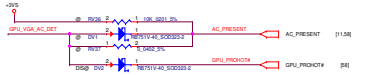
Date: Thursday, March 31, 2022 | Sheet 29 of 120

GPIO

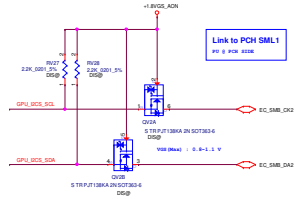
I2CS SMBUS: 0x9E and 0x9C (Default)

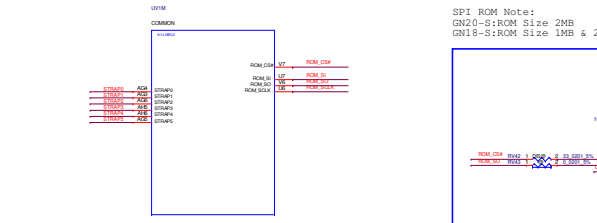




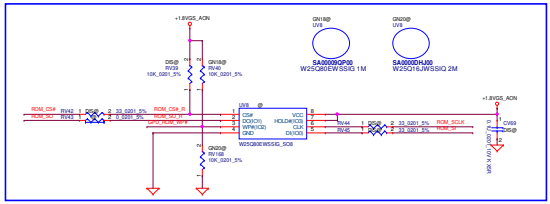


Internal Thermal Sensor

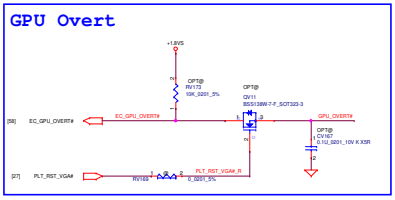




SPI ROM Note:
GN20-S:ROM Size 2MB
GN18-S:ROM Size 1MB & 2MB



GPU Overt



STRAP

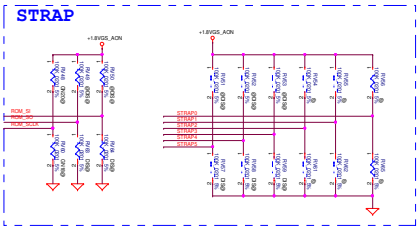


Table Number	STRAP 2	STRAP 1	STRAP 0	Vendor	Vendor P/N	Die Type	Memory Capacity	COMPAL P/N	X76
0	L	L	L	Samsung	K4Z80325BC-HC14	C-Die	1GB	SA0000C6260	[redacted]
1	L	L	H						[redacted]
2	L	H	L	Hynix	H56CBH24AIR-S2C	A-Die	1GB	SA0000DUW00	[redacted]
3	L	H	H						[redacted]
4	H	L	L						[redacted]
5	H	L	H	Hynix	H56G32CS4DX005	C-Die	1GB	TBD	[redacted]
6	H	H	L						[redacted]
7	H	H	H	Micron	MT61K512M32KPA-14:C	C-Die	2GB	TBD	[redacted]
8	L	L	M	Hynix	H56G42AS2DX014	A-Die	2GB	TBD	[redacted]
9	L	M	L	Samsung	K4ZAF325BM-HC14	M-Die	2GB	SA0000CBG00	[redacted]
10	L	M	H						[redacted]
11	L	H	M						
12	M	L	L						
13	M	L	H						
14	M	H	L						
15	M	H	H						

Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SDV build		STRIP 2	STRIP 1	STRIP 0
Samsung K4Z80325BC-HC14	VRAM_S1G@	L	L	L
Hynix H56G32CS4DX005	VRAM_H1G@	H	L	H
Samsung K4ZAF325BM-HC14	VRAM_S2G@	L	M	L

Ternary Straps

Table 4 summarizes the ternary strap mapping for the GB3-64 GPUs and the GB3B-64 GPUs.

Table 4. GB3-64 and GB3B-64 Ternary Straps

Strap Pin	GB3-64	GB3B-64
ROM_SI ROM_SO ROM_CLK	Set {ROM_SO, ROM_SI, ROM_CLK} to {L, L, H} to enable FS_OVERT* • ROM_SI and ROM_CLK: 100 kΩ • ROM_SO: 10 kΩ	Set {ROM_SO, ROM_SI, ROM_CLK} to {L, L, L} to enable FS_OVERT • ROM_SI and ROM_CLK: 100 kΩ • ROM_SO: 10 kΩ
STRAP5	• SMB_ALT_ADDR	• SMB_ALT_ADDR

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			Date: Tuesday, January 25, 2022 Sheet 30 of 130

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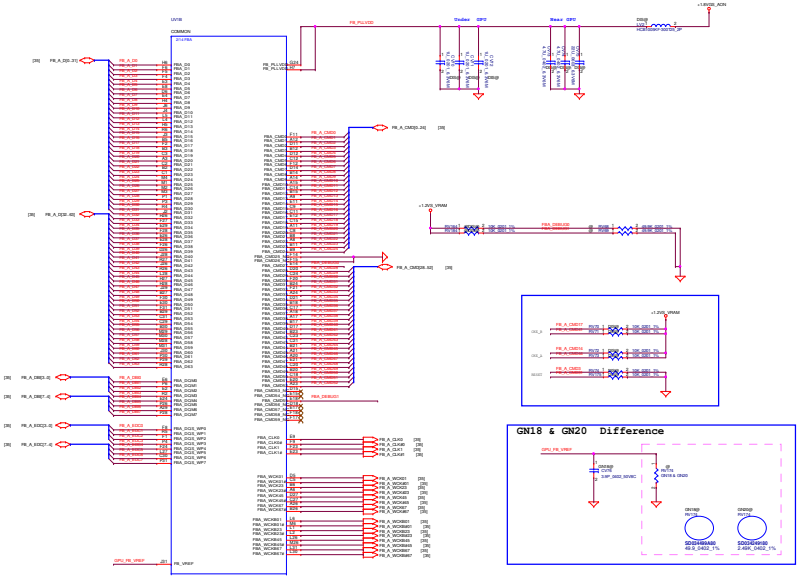

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Size	Document Number	Rev
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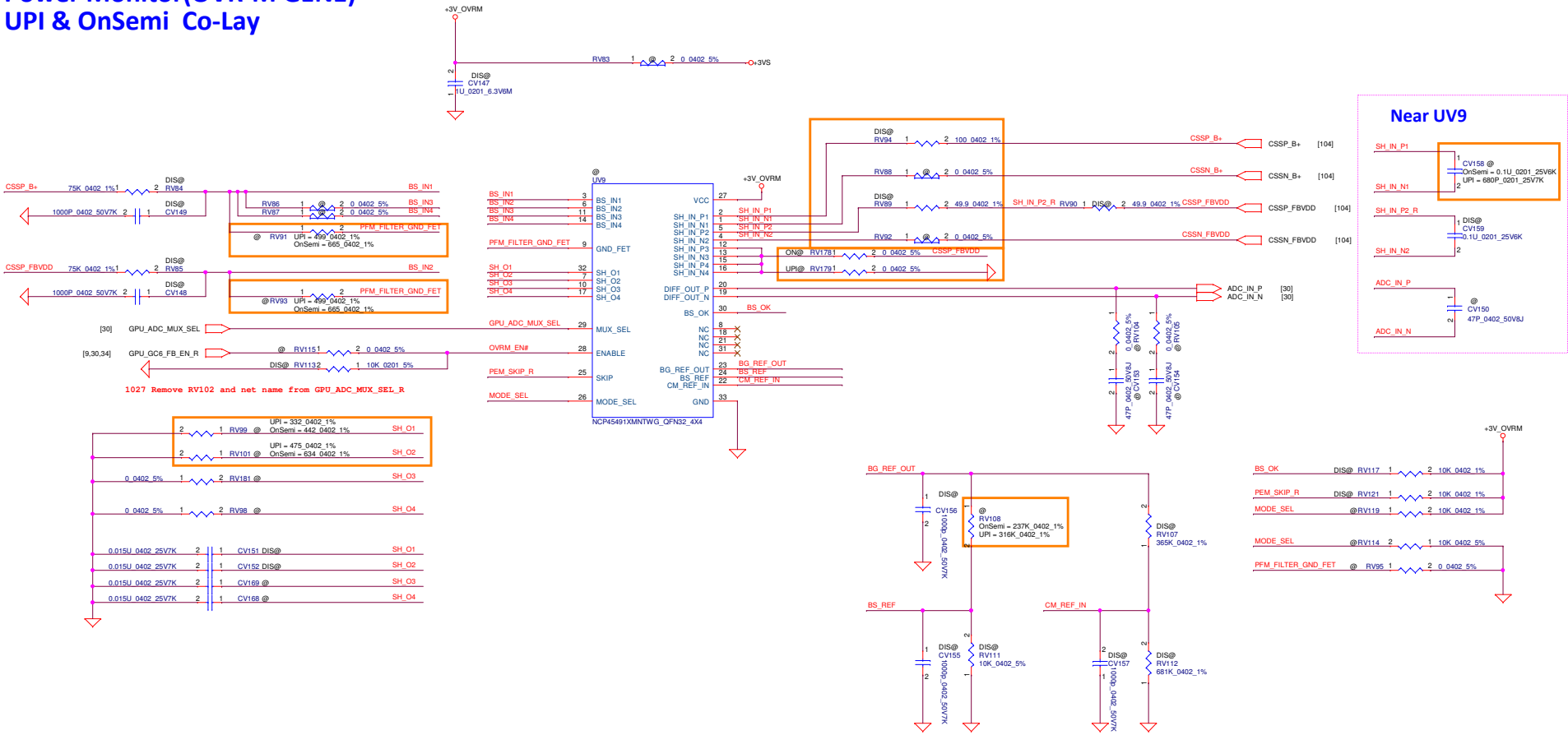
Date: Tuesday, January 25, 2022 | Sheet 32 of 120

Power Monitor(OVR-M GEN1)
UPI & OnSemi Co-Lay



UPI & ONSEMI BOM Structure

UPI	UPI@ UV9 SA0000CMA00 US5650QQKI	UPI@ RV91 SD034499080 499_0402_1%	UPI@ RV93 SD034499080 499_0402_1%	UPI@ RV101 SD034475080 475_0402_1%	UPI@ RV99 SD034332080 332_0402_1%	UPI@ RV108 SD034316380 316K_0402_1%	UPI@ CV158 SE00000WY80 680P_0201_25V7K
ONSEMI	ON@ UV9 SA0000CQX00 NCP45492	ON@ RV91 SD00000JJ00 665_0402_1%	ON@ RV93 SD00000JJ00 665_0402_1%	ON@ RV101 SD00000Z280 634_0402_1%	ON@ RV99 SD034442080 442_0402_1%	ON@ RV108 SD034237380 237K_0402_1%	ON@ CV158 SE00001AA00 0.1U_0201_25V6K

Part Reference	UPI	OnSemi
RV92	0_0402_5%	49.9_0402_1%
RV88	0_0402_5%	49.9_0402_1%
RV94	100_0402_1%	49.9_0402_1%
RV108	316K_0402_1%	237K_0402_1%
RV99	332_0402_1%	442_0402_1%
RV101	475_0402_1%	634_0402_1%
RV89	49.9_0402_1%	0_0402_5%
RV93	499_0402_1%	665_0402_1%
RV91	499_0402_1%	665_0402_1%
CV158	680P_0201_25V7K	0.1U_0201_25V6K

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			Size: C Document Number: LA-L931P Rev: 1.0
			Date: Thursday, April 21, 2022 Sheet 33 of 120

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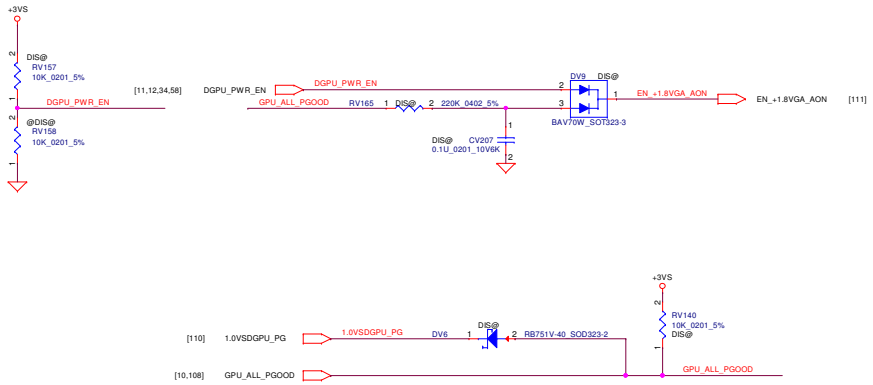
GPU_1.8V Enable
1.8VS->+1.8VGS_AON

+1.8VS to +1.8VGS_AON

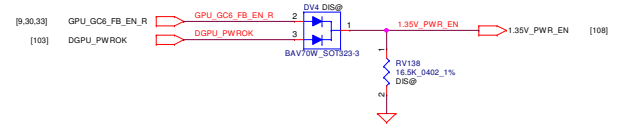


GC6 Mode Hold FBVDD Power rail

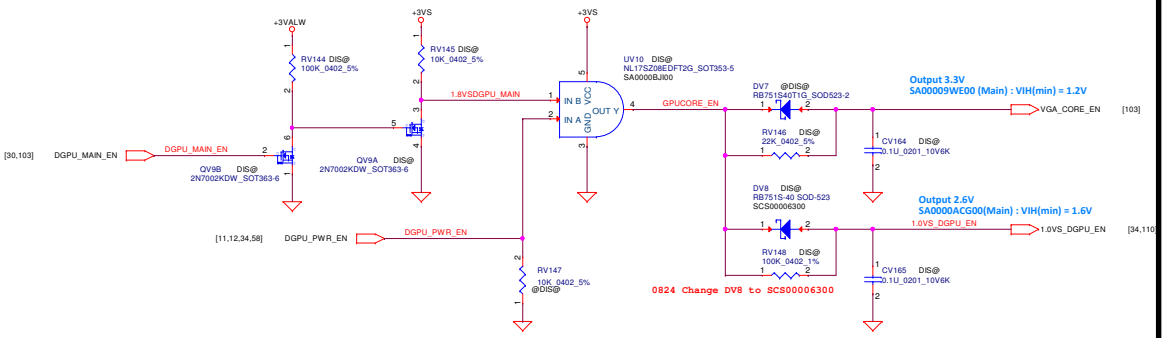
GC6 Mode Hold FBVDD Power rail

For GC6

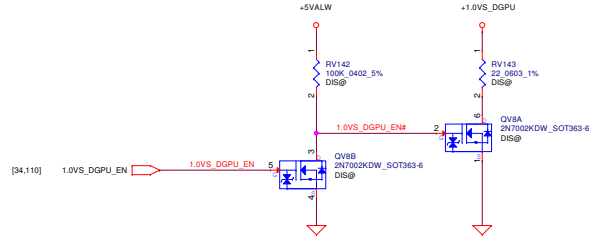
Normal:1.8V
GC6:1.3V
SA000099200 (Main) : VIH(min) = 0.8V
SA000081400 (2nd) : VIH(min) = 0.8V

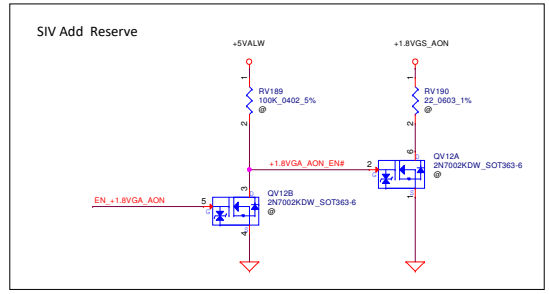


VGA_CORE_EN & 1.0VS_DGPU_EN



1.0VS_DGPU Discharge





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Size	Document Number		Rev
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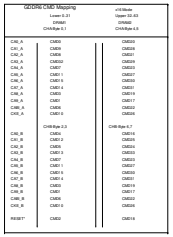
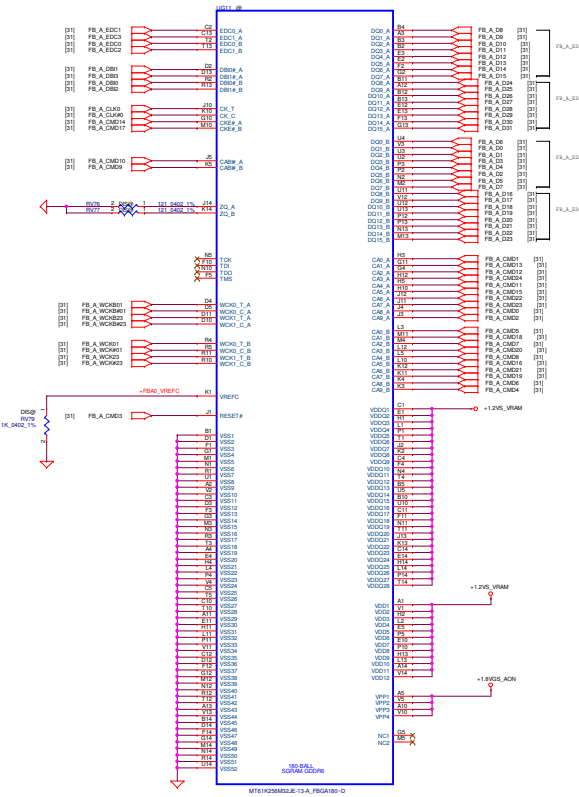
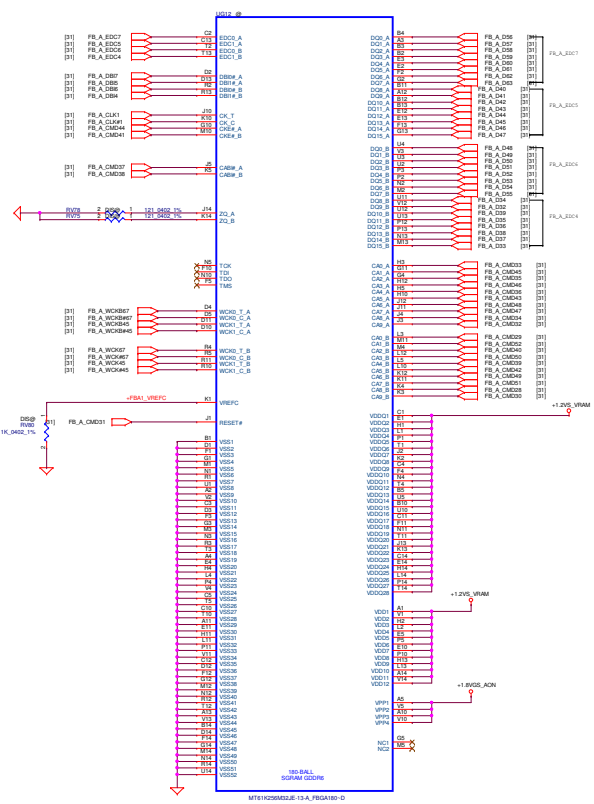
Date:	Tuesday, March 29, 2022	Sheet 34 of 120	

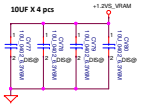
VRAM A



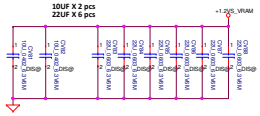




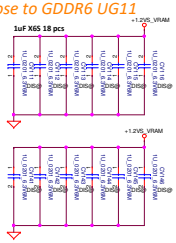
Close to GDDR6 UG11



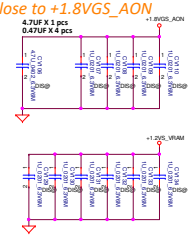
Around GDDR6 UG11



Close to GDDR6 UG11

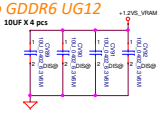


Close to +1.8VGS_AON

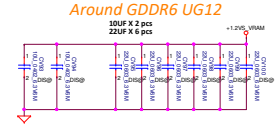


VRAM		BOM structure	UG11	UG12
GDDR6 14Gbps 8Gb	Hynix H56G32CS4DX005	VRAM_H1G@	SA0000ENP20 Hynix H56G32CS4DX005	SA0000ENP20 Hynix H56G32CS4DX005
	Samsung K4280325BC-HC14	VRAM_S1G@	SA0000C6270 Samsung K4Z80325BC-HC14	SA0000C6270 Samsung K4Z80325BC-HC14
GDDR6 14Gbps 16Gb	Samsung K4ZAF325BM-HC14	VRAM_S2G@	SA0000CBG70 Samsung K4ZAF325BM-HC14	SA0000CBG70 Samsung K4ZAF325BM-HC14
	Hynix H56G42AS4DX014	VRAM_H2G@	SA0000EPM10 Hynix H56G42AS4DX014	SA0000EPM10 Hynix H56G42AS4DX014
	Micron MT61K512M32KPA-14:C	VRAM_M2G@	SA0000ERM00 Micron MT61K512M32KPA-14:C	SA0000ERM00 Micron MT61K512M32KPA-14:C

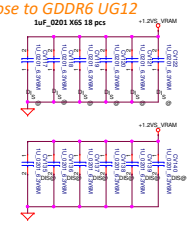
Close to GDDR6 UG12



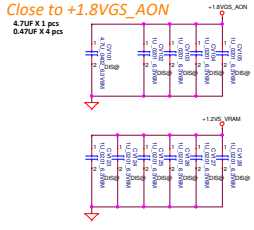
Around GDDR6 UG12



Close to GDDR6 UG12



Close to +1.8VGS_AON



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Issued Date	2021/10/12	Deciphered Date 2021/10/12	Title	P035-GDDR6
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			Date: Tuesday, February 08, 2022	Sheet 35 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve for N16P_GDDR5_A_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 36 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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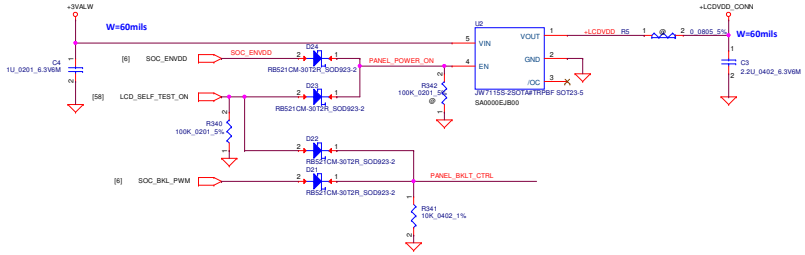
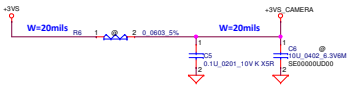
Compal Electronics, Inc.		
Title: *DGPU_DC/DC Interface_EE*		
Size	Document Number: *LA-L931P*	Rev: 1.0
Date: Tuesday, January 25, 2022	Sheet 37 of 120	

LCD POWER SWITCH



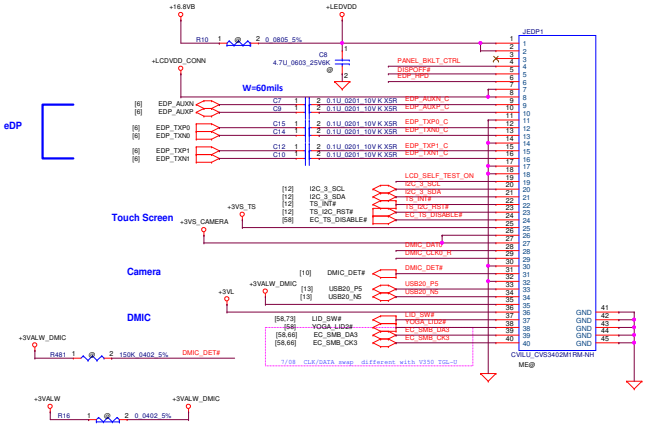
CAMERA POWER CIRCUIT



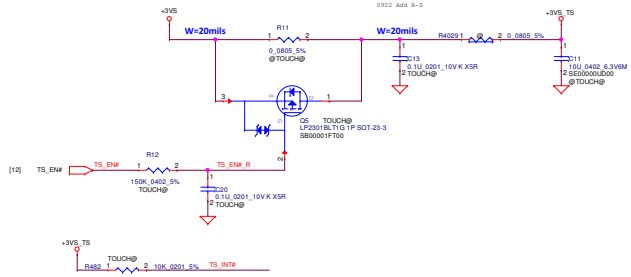
DISPLAY OFF

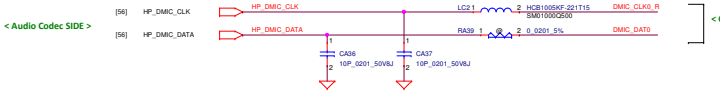
HOT PLUG DETECT

eDP CONNECTOR



Touch Screen POWER CIRCUIT





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Issued Date	2021/10/12	Deciphered Date	2021/10/12

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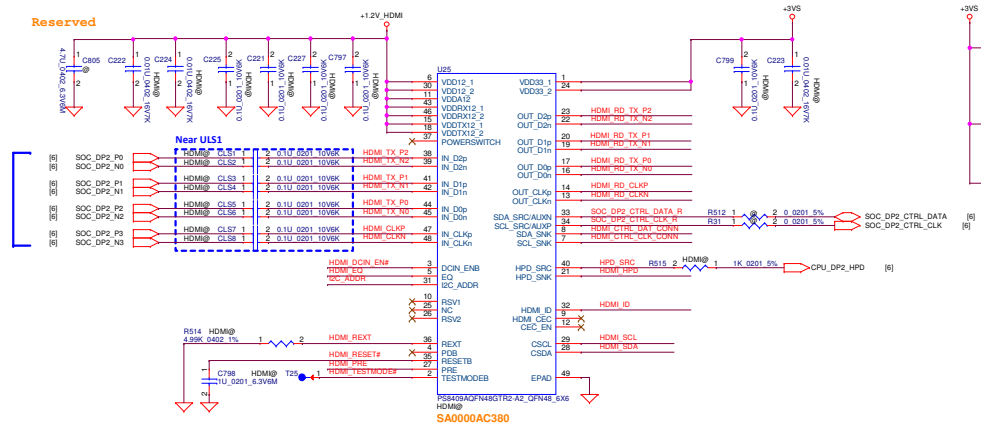
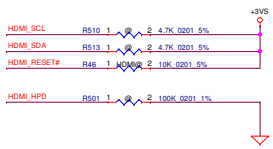
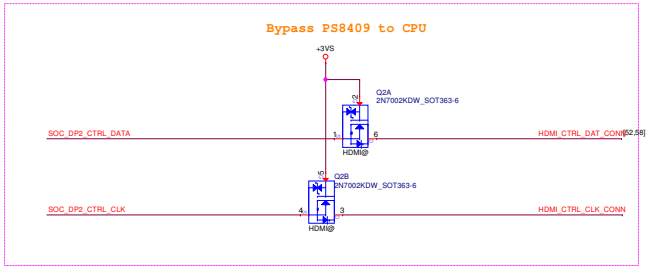
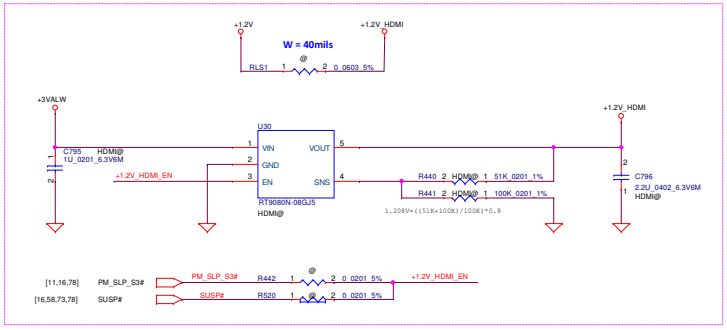
Compal Electronics, Inc.	
Title	eDP / DMIC / IR Camera / Touch EE
Size	Document Number: LA-L931P
Rev	1.0
Date:	Wednesday, August 31, 2022
Sheet	38 of 126

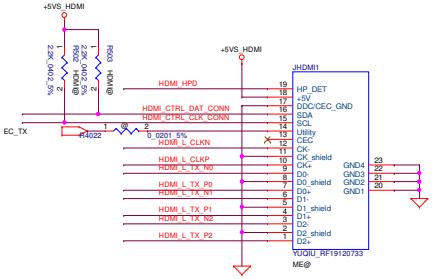
HDMI 2.0_PS8409A

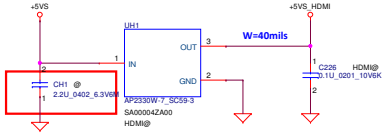


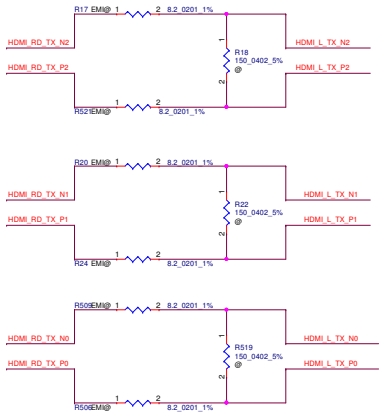


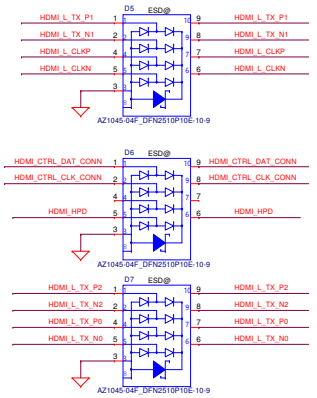












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Compal Electronics, Inc.			
Title: P039-HDMI 2.0			
Size	Document Number: LA-L931P		Rev: 1.0
Date: Thursday, March 31, 2022	Sheet 39 of 120		

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **CloverFalls Conn_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 40 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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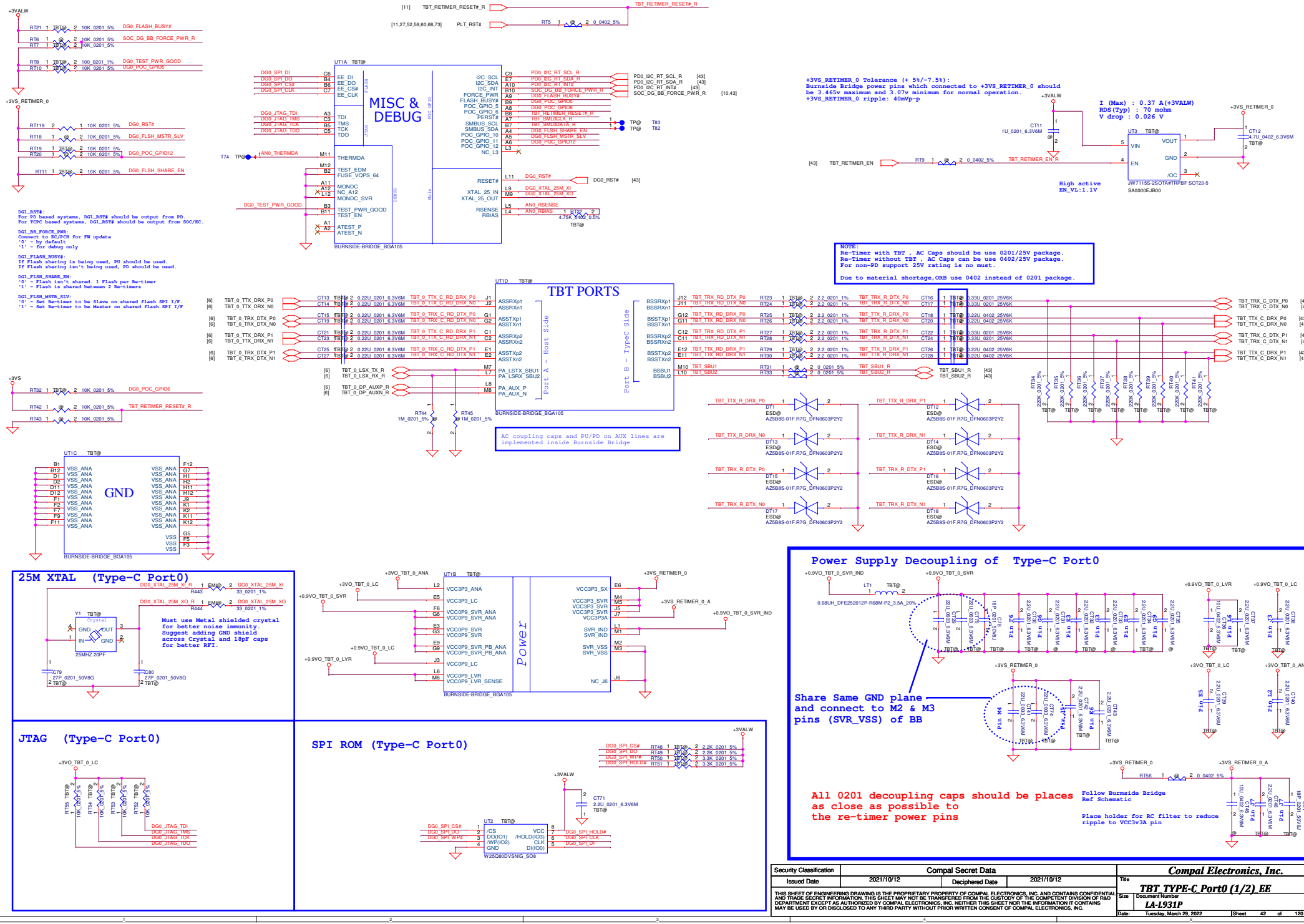
Compal Electronics, Inc.

Title: **Reserve for CRT_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 41 of 120

MB_USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)



Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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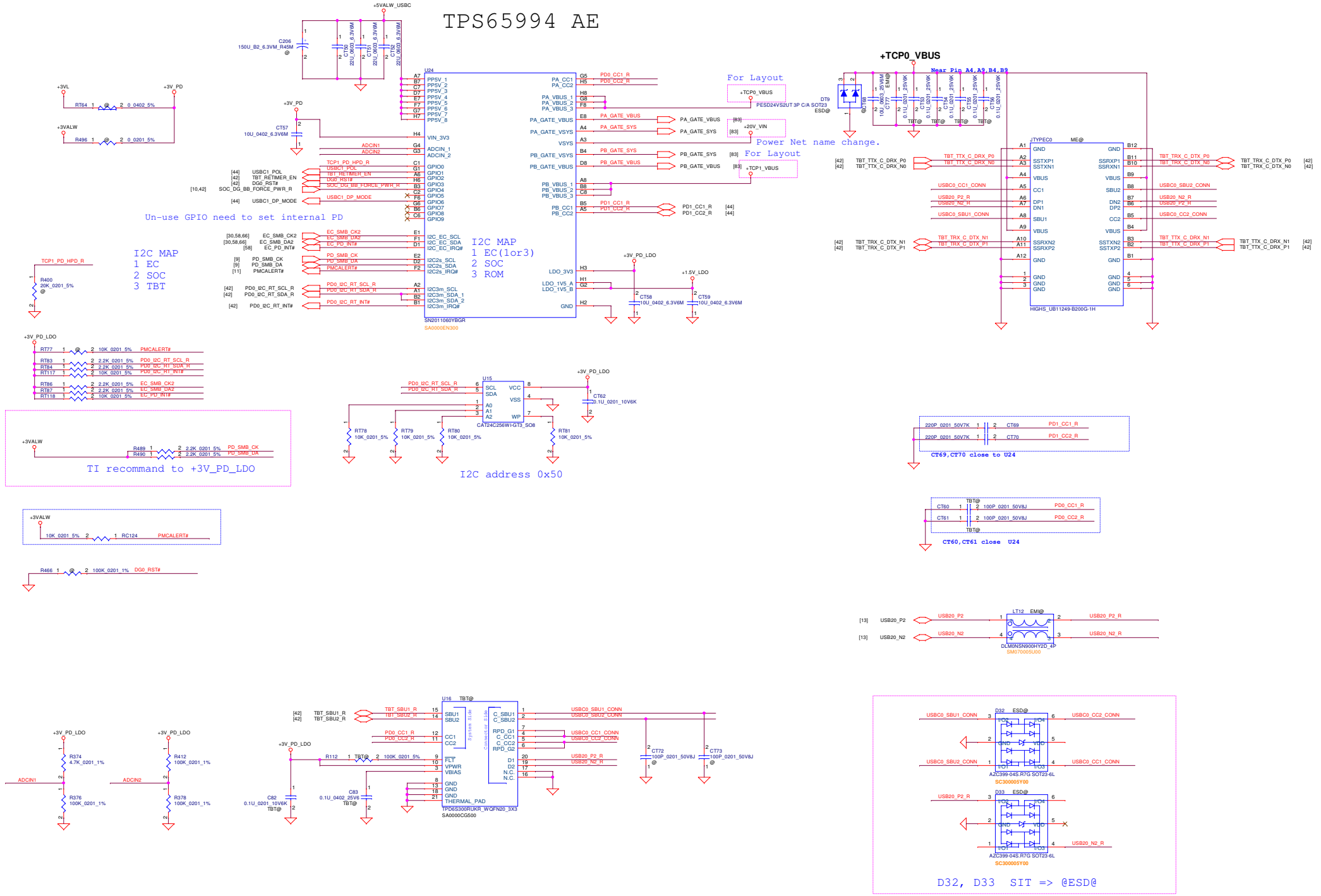
Compal Electronics, Inc.	
Title	TBT TYPE-C Port0 (1/2) EE
Size	Document Number: LA-L931P
Rev	1.0
Date:	Tuesday, March 29, 2022
Sheet	42 of 120

TPS65994 AE



Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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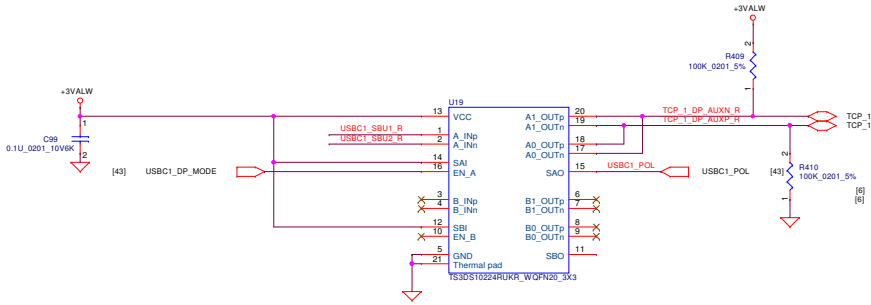
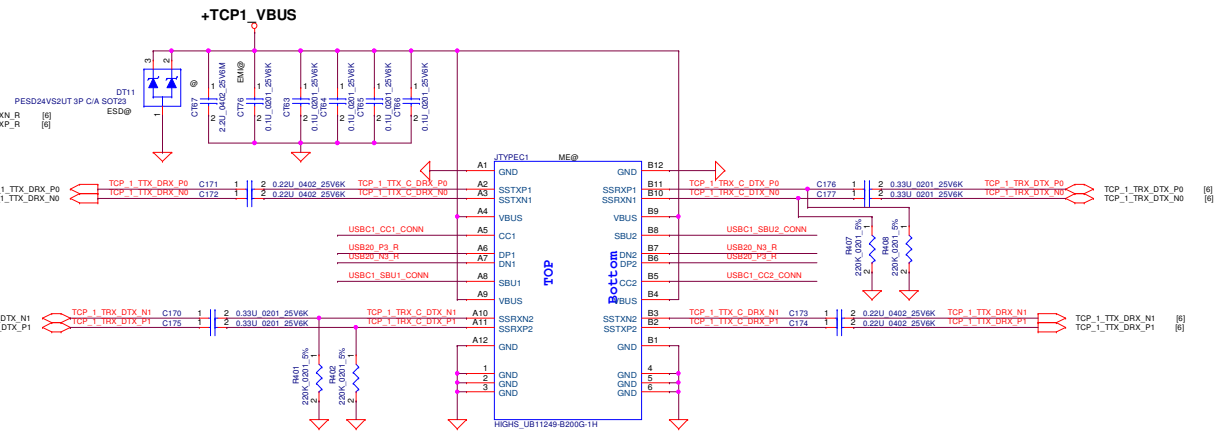
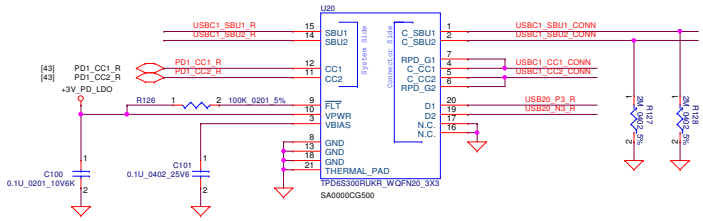
Compal Electronics, Inc.	
Title	TBT TYPE-C Port0 (2/2) EE
Size	Document Number: LA-L931P
Rev	1.0
Date:	Tuesday, March 29, 2022
Sheet	43 of 120

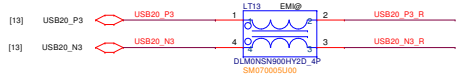
Type-C PORT 1

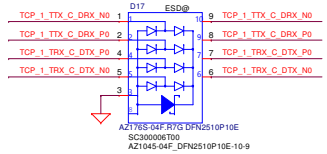


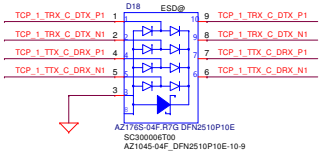


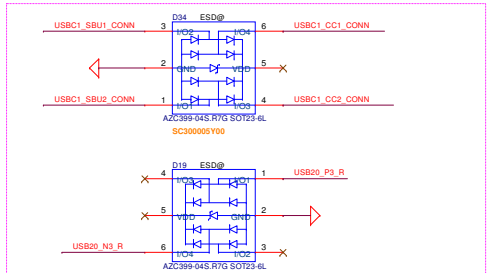
SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	–	INA	–
0001	INB	–	–	INA
0010	INB	–	INB	–
0011	INB	–	–	INB
0100	–	INB	INA	–
0101	–	INB	–	INA
0110	–	INB	INB	
0111	–	INB	–	INB
1000	INA	–	INA	–
1001	INA	–	–	INA
1010	INA	–	INB	–
1011	INA	–	–	INB
1100	–	INA	INA	–
1101	–	INA	–	INA
1110	–	INA	INB	–
1111	–	INA	–	INB











Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.			
Title: TBT TYPE-C Port1 (1/2) EE			
Size	Document Number: LA-L931P		Rev: 1.0
Date: Tuesday, January 25, 2022	Sheet 44 of 120		

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **TBT_TYPE-C Port1 (2/2) EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 45 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **TBT_TYPE-C Port2 (1/2) EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 46 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **TBT TYPE-C Port2 (2/2) EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 47 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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	Compal Electronics, Inc.	
Title	***TBT TYPE-C Port3 (1/2) EE***	
Size	Document Number	Rev
	LA-L931P	1.0
Date:	Tuesday, January 25, 2022	Sheet 48 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve for TBT_TYPE-C Port3 (2/2) EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 49 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **TYPE-C Power Path_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 50 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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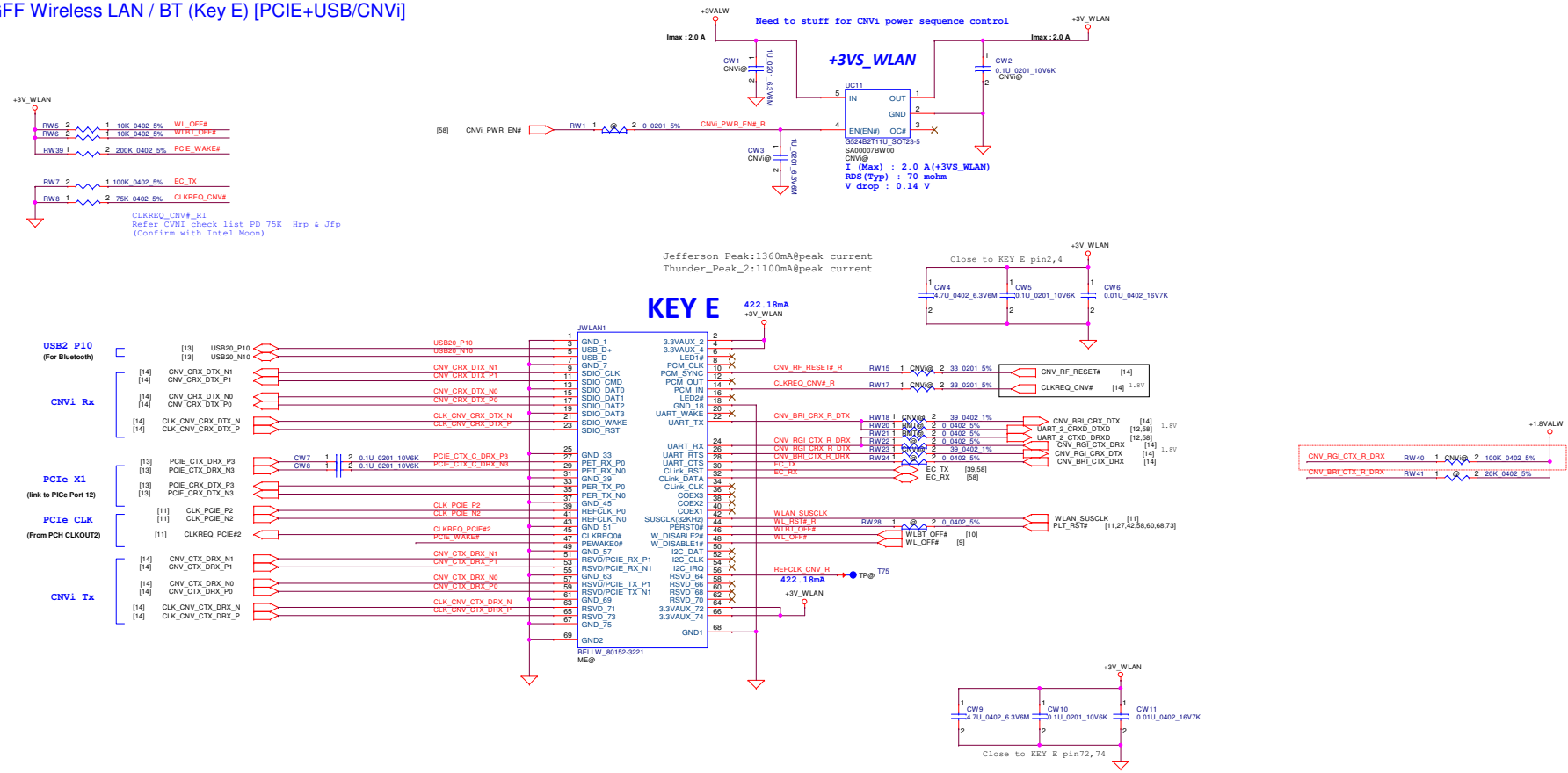
Compal Electronics, Inc.

Title: **LAN-RTL8111H EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 51 of 120

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.	
Title	NGFF WL(KEY E) / WWAN(KRY EE
Size	Document Number: LA-L931P
Rev	1.0
Date:	Wednesday, August 31, 2022
Sheet	52 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve for WIGIG/WIDI EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 53 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve for PCIE Device EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 54 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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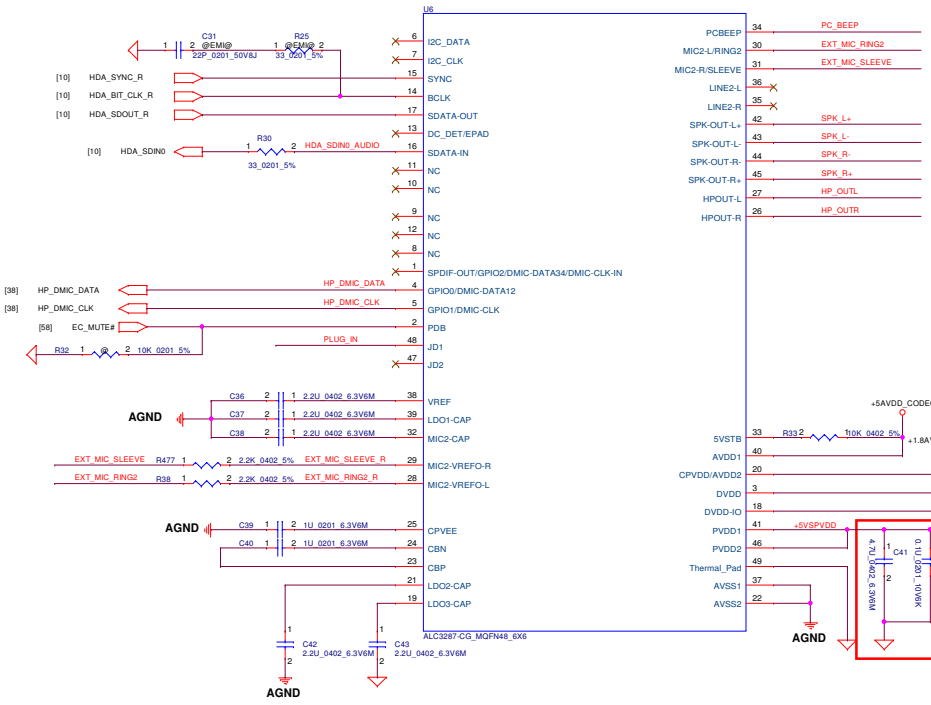
Compal Electronics, Inc.

Title: **Reserve for PCIE Device EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 55 of 120

ALC3287

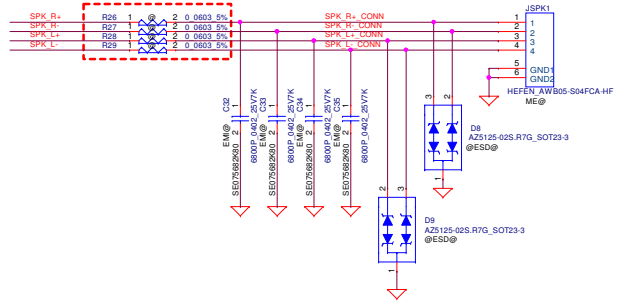


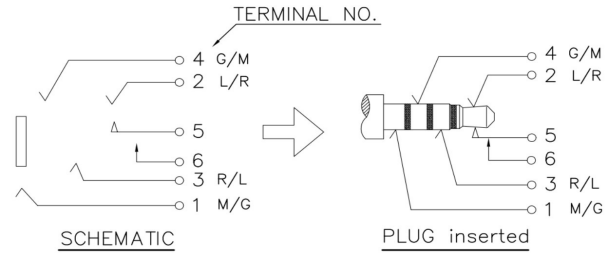
Speaker

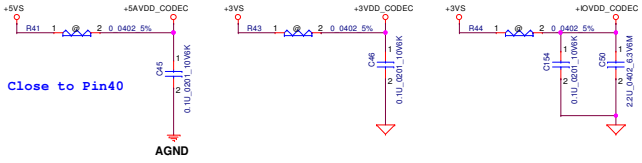
wide 40MIL

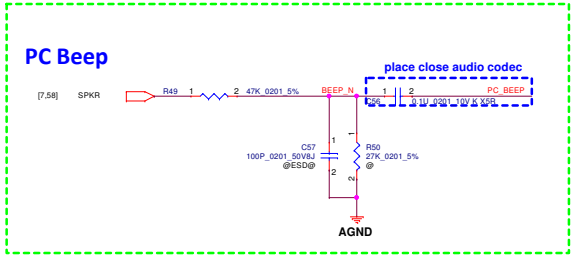
Speaker Connector PN SP020015V00

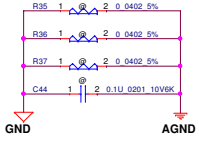
EMI







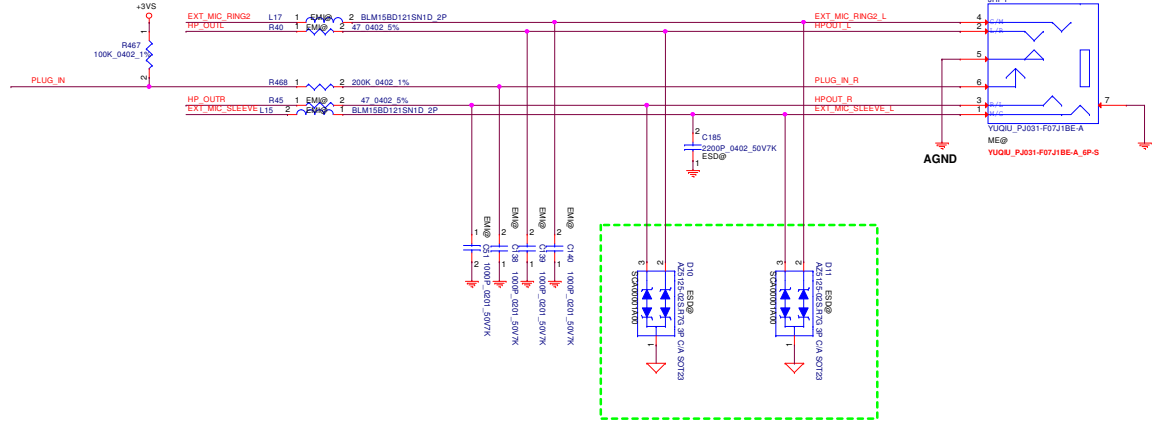




wide 60MIL

Combo Jack (Normal Open)

W=40mils



Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.	
Title	Audio ALC256&711/Audio Conn EE
Size	Document Number: LA-L931P
Rev	1.0
Date:	Thursday, March 31, 2022
Sheet	56 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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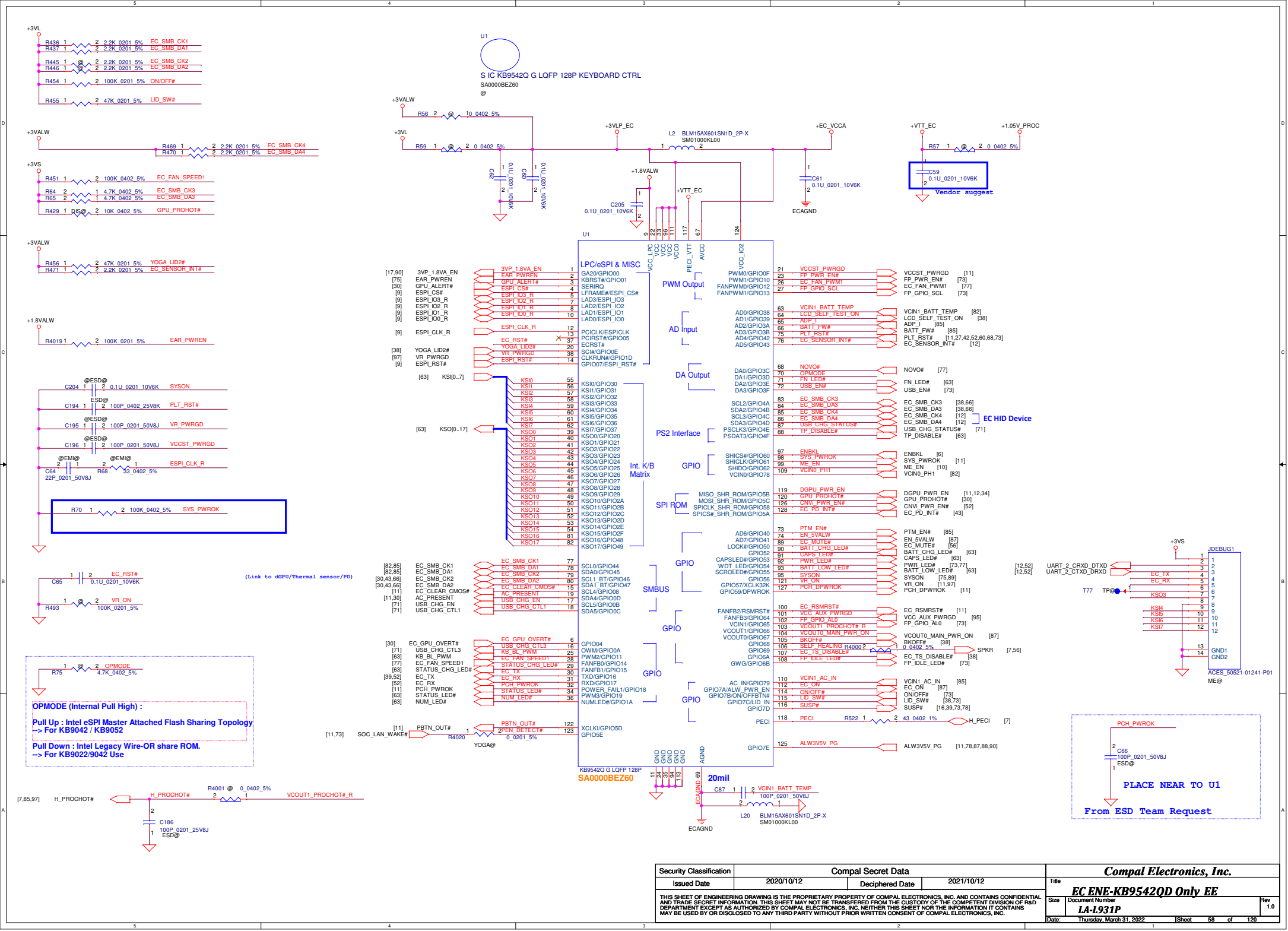
Compal Electronics, Inc.

Title: **Reserve for Audio Ampfilper EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 57 of 120



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Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: EC ENE-KB9542QD Only EE

Size	Document Number	Rev
	LA-L931P	1.0

Date: Thursday, March 31, 2022 | Sheet 58 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

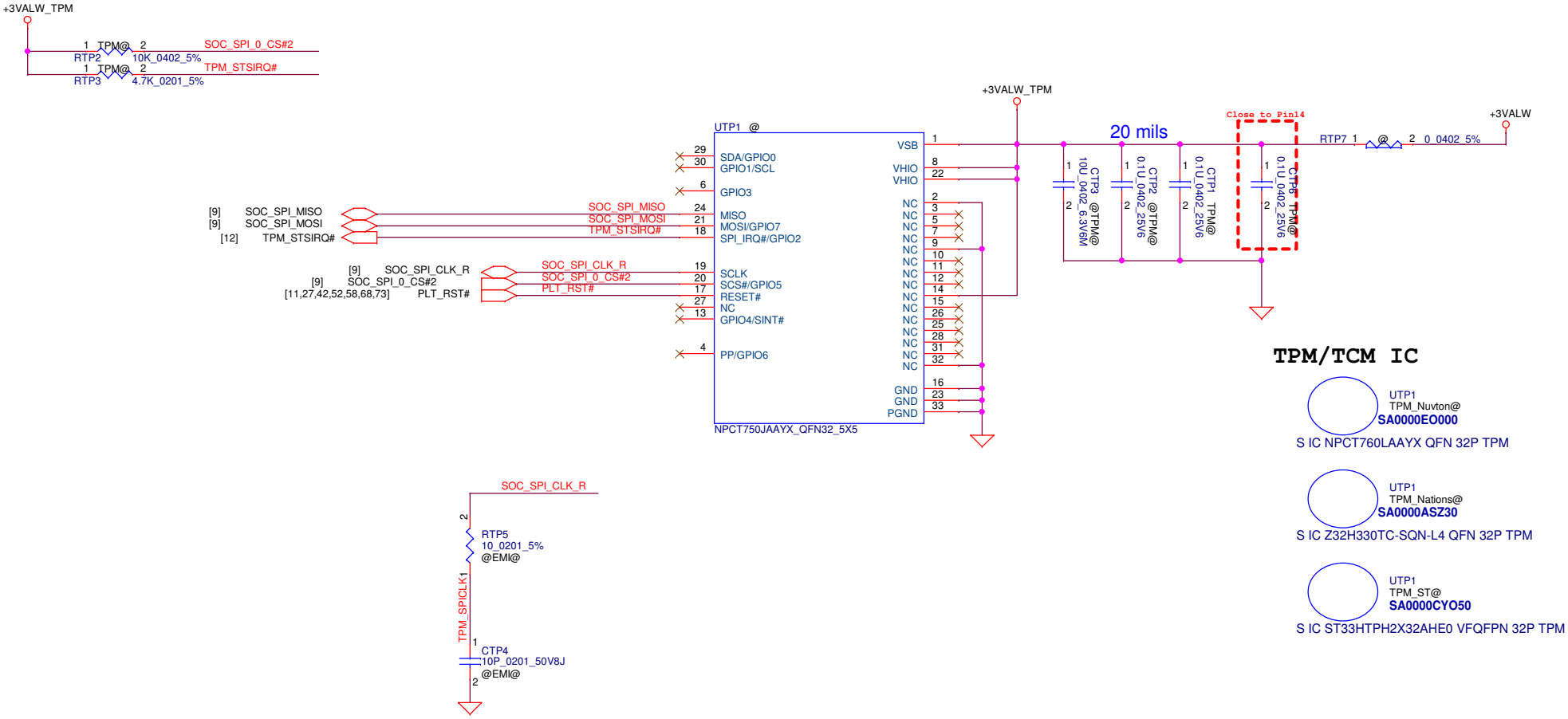
Title: **Reserve for KBC&SIO_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 59 of 120

TPM 2.0 Co-lay

1.Nuvton_NPCT750LABYX
2.ST_ST33HTPH2E32AAE8
3.Nations_Z32H330TC



TPM/TCM IC

UTP1
TPM_Nuvton@
SA0000EO000
S IC NPCT760LAAYX QFN 32P TPM

UTP1
TPM_Nations@
SA0000ASZ30
S IC Z32H330TC-SQN-L4 QFN 32P TPM

UTP1
TPM_ST@
SA0000CYO50
S IC ST33HTPH2X32AHE0 VFQFPN 32P TPM

Security Classification	Compal Secret Data		
Issued Date	2020/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve for Secure & Reset IC_EE**

Size | Document Number: **LA-L931P** | Rev: 1.0

Date: Thursday, March 31, 2022 | Sheet 60 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve for SMB/I2C Block Diagrams_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 61 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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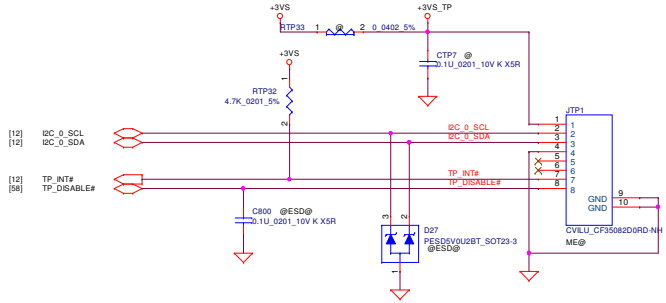
Compal Electronics, Inc.

Title: **Reserve for LEDs Controller_EE**

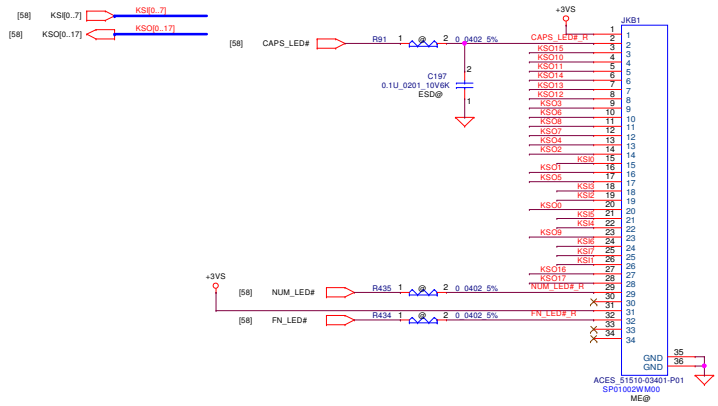
Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 62 of 120

Touch Pad

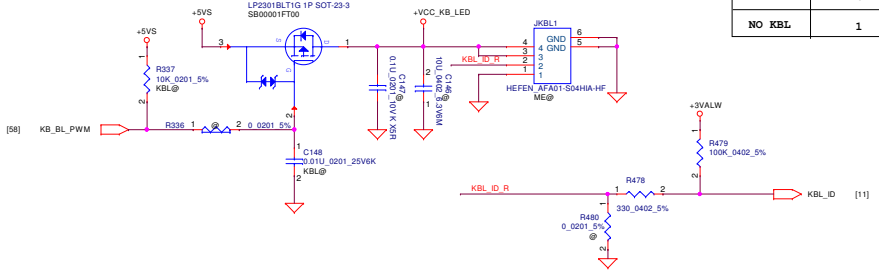


Keyboard

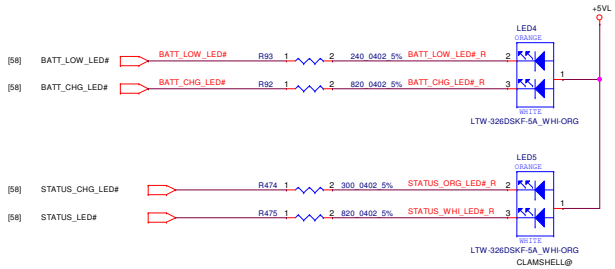


Keyboard Backlight

Function	KBL_ID
KBL	0
NO KBL	1



BATT LED



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Compal Electronics, Inc.			
Title	KB/TP/LED/LID_EE		
Size	Document Number		Rev
	LA-L931P		1.0
Date:	Thursday, March 31, 2022	Sheet	63 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve for KB/TP/LED/LID EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 64 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

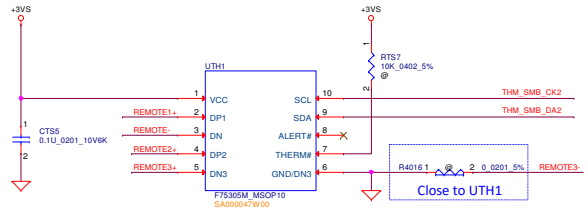
Title: **Reserve for KB/TP/LED/LID_EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 65 of 120

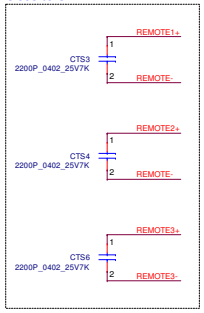
Thermal sensor

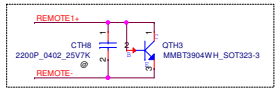
3V/5V sensor for IO port loading



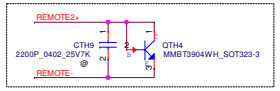
Address 1001_101xb

Close to UTH1

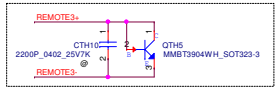




CPU Choke



Charger CHOKE

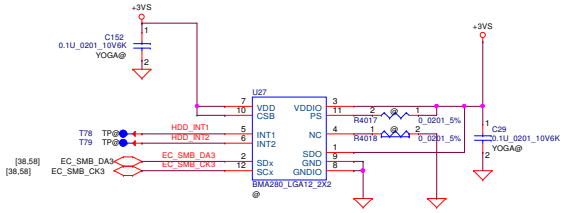


thermal sensor for lid

REMOTE1,2,3 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

LIS2DWLTR for APS => Titan 3.0 no support APS

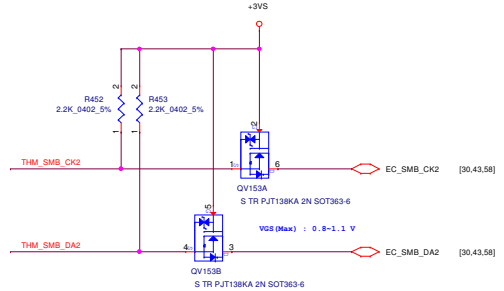
BMA253 for YOGA G-Sensor



1027 Change R4018 to short pad

I2C Address: 0011001b 0x19

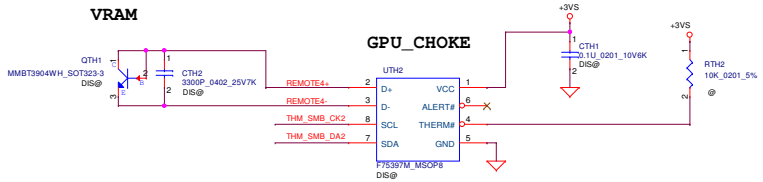
	R4015	R4017	R4018	
ST LIS2DWL		@		default
BMA422		@	@	



Reserved

VRAM

GPU_CHOKE



Address 1001_100xb

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.	
Title	Sensor/Finger Print_EE
Size	Document Number: LA-L931P
Rev	1.0
Date:	Tuesday, March 29, 2022
Sheet	66 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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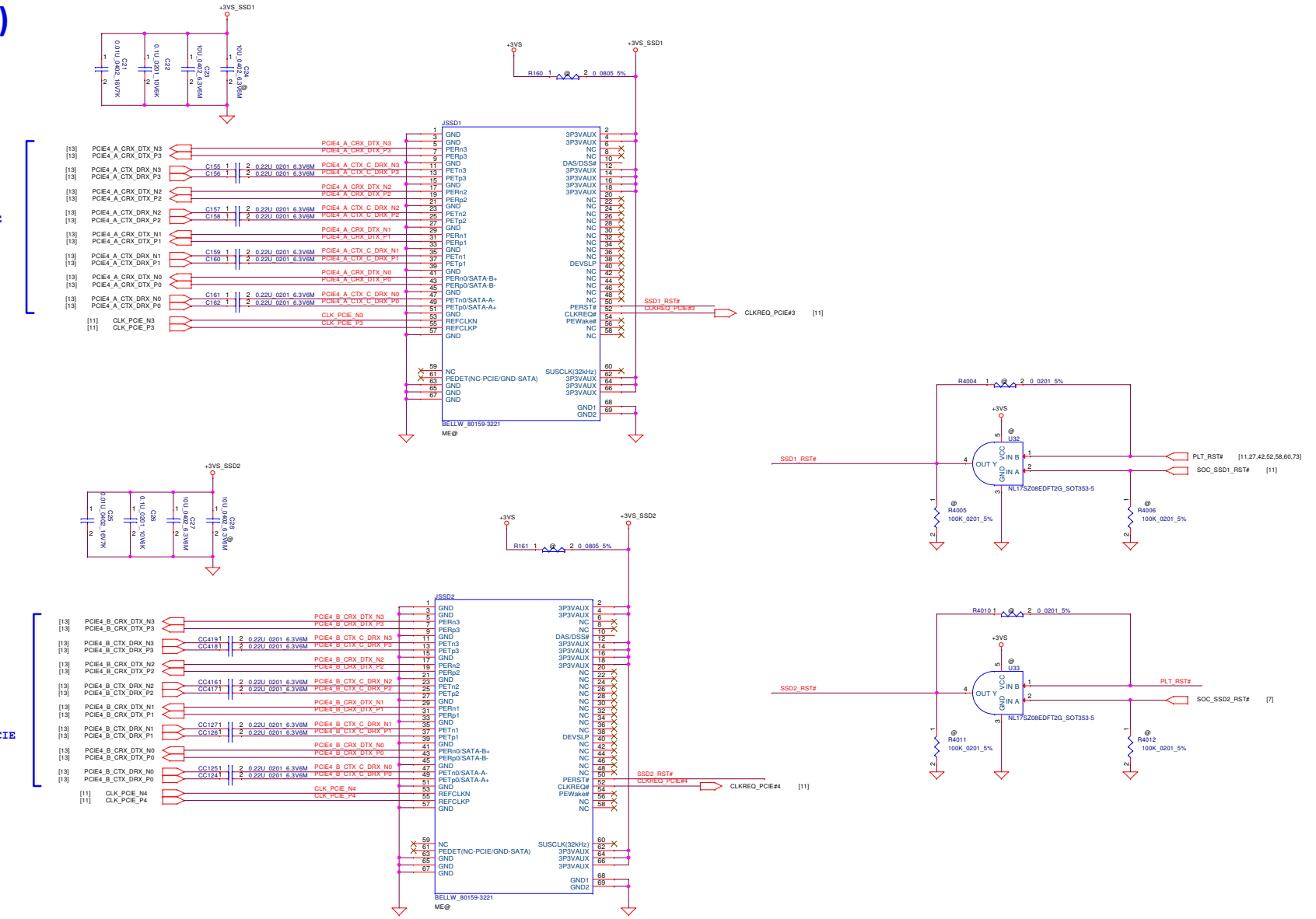
Compal Electronics, Inc.

Title: **HDD/ODD Connector EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 67 of 120

SSD(TYPE M)



Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.			
Title	NGFF SSD(KEY M) EE		
Size	Document Number		Rev
	LA-L931P		1.0
Date:	Thursday, March 31, 2022	Sheet	68 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **Reserve eMMC EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 69 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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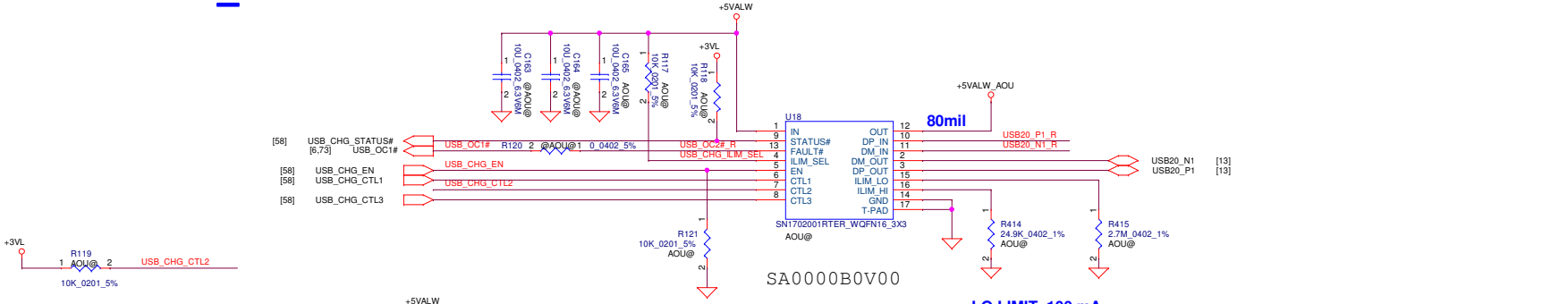
Compal Electronics, Inc.

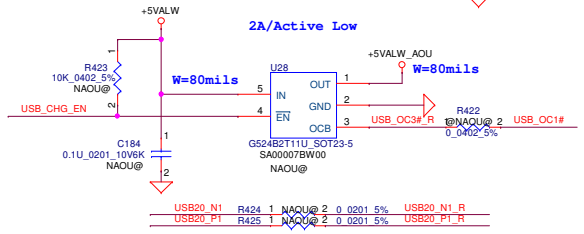
Title: **Card Reader RTS5227S EE**

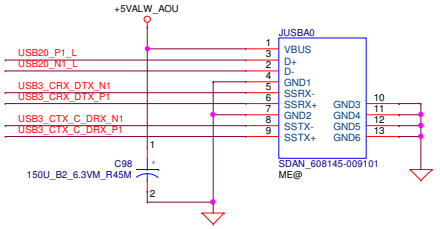
Size	Document Number	Rev
	LA-L931P	1.0

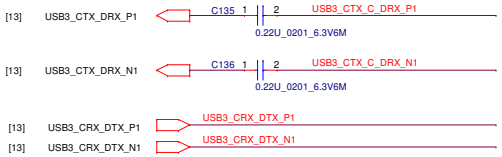
Date: Tuesday, January 25, 2022 | Sheet 70 of 120

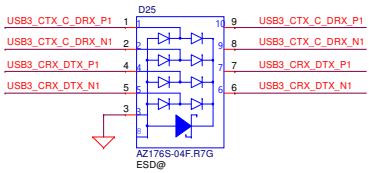
USB3.0_Port0 AOU

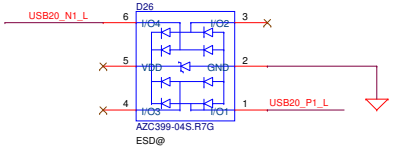


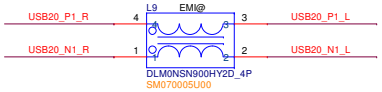












Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.			
Title	USB2/USB3 TYPEA1&2 EE		
Size	Document Number		Rev
	LA-L931P		1.0
Date:	Tuesday, January 25, 2022	Sheet	71 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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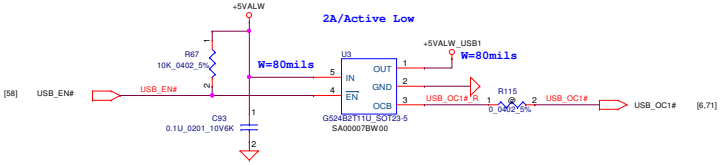
Compal Electronics, Inc.

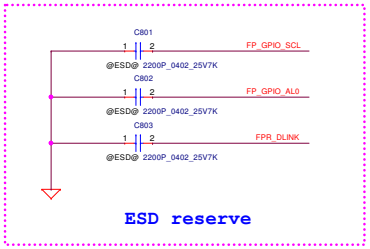
Title: **Reserve USB2/USB3 TYPEA EE**

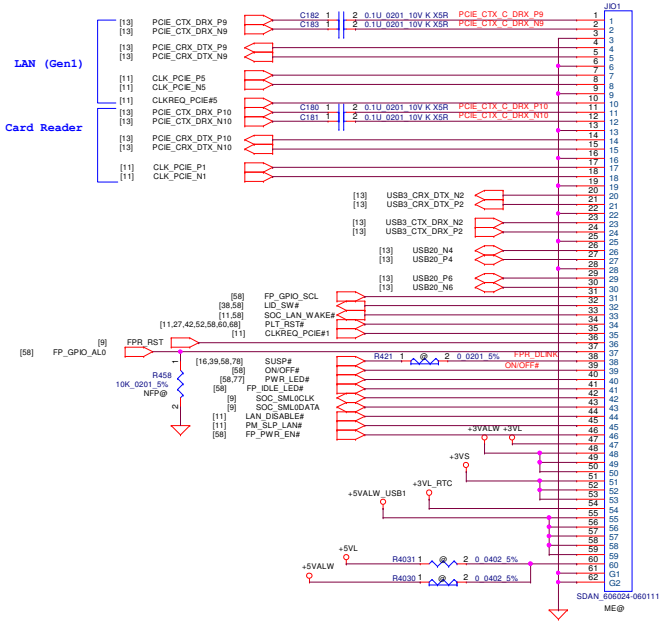
Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 72 of 120

USB3.0_Port1 SW







Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.			
Title: Reserve USB2/USB3 DB_EE			
Size	Document Number: LA-L931P		Rev: 1.0
Date: Thursday, March 31, 2022	Sheet 73 of 120		

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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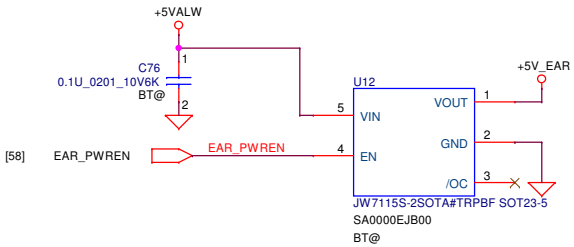
Compal Electronics, Inc.

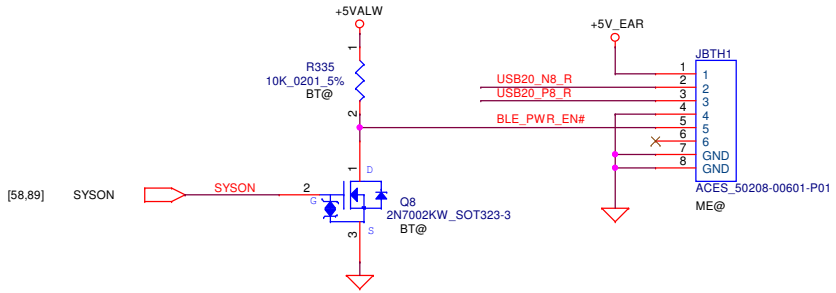
Title: **Reserve for Dock EE**

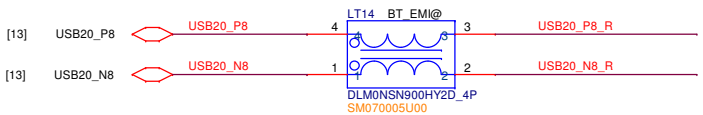
Size	Document Number	Rev
	LA-L931P	1.0

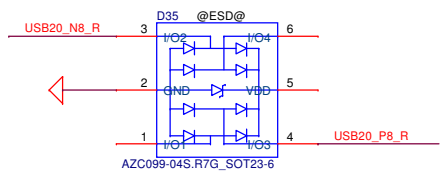
Date: Tuesday, January 25, 2022 | Sheet 74 of 120

BT head phone









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Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: Reserve for USB_EE

Size | Document Number: LA-L931P | Rev: 1.0

Date: Tuesday, January 25, 2022 | Sheet 75 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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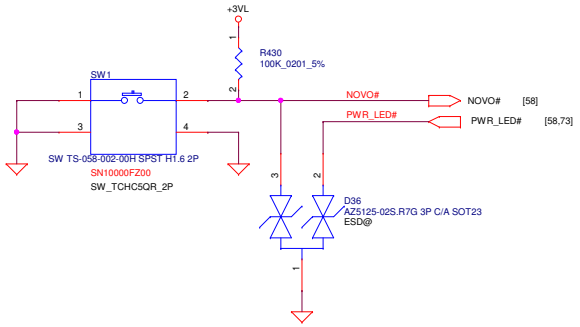
Compal Electronics, Inc.

Title: **Reserve for USB_EE**

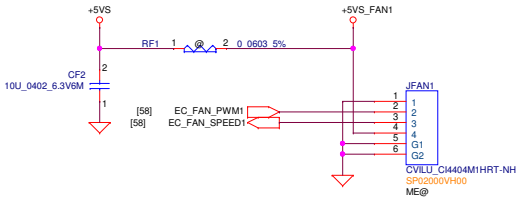
Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 76 of 120

NOVO Button

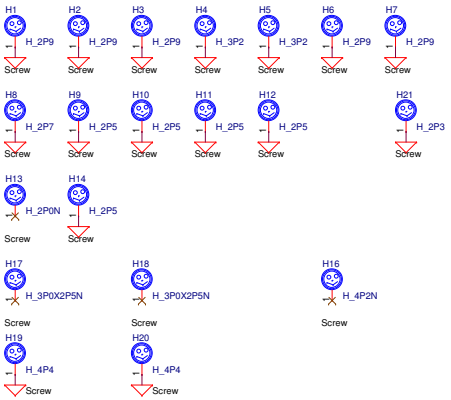


CPU Fan Control Circuit



PCB	ZZZ PCB 3SE LA-L932P REV0 M/B 2 S DA8001SQ000 LA_L932P@ **Not Use**	ZZZ PCB 3SD LA-L931P REV0 M/B 2 S DA8001SL010 LA_L931P@
DDR	DDR 4G ZZZ ALT. GROUP PARTS DRAM 4G SAM X7695138001 X76_DDR_SAM_4G@ ZZZ ALT. GROUP PARTS DRAM 4G HYNIX X7695138002 X76_DDR_HYN_4G@ ZZZ ALT. GROUP PARTS DRAM 4G MICRON X7695138003 X76_DDR_MIC_4G@	DDR 8G ZZZ ALT. GROUP PARTS DRAM 8G SAM X7695138004 X76_DDR_SAM_8G@ ZZZ ALT. GROUP PARTS DRAM 8G HYNIX X7695138005 X76_DDR_HYN_8G@ ZZZ ALT. GROUP PARTS DRAM 8G Micron X7695138016 X76_DDR_MIC_8G@
VRAM	ZZZ ALT. GROUP PARTS VRAM 2G HYNIX X7695138006 X76_VRAM_HYN_2G@ ZZZ ALT. GROUP PARTS VRAM 2G SAM X7695138007 X76_VRAM_SAM_2G@	ZZZ ALT. GROUP PARTS VRAM 4G HYNIX X7695138009 X76_VRAM_HYN_4G@ ZZZ ALT. GROUP PARTS VRAM 4G SAM X7695138008 X76_VRAM_SAM_4G@ ZZZ ALT. GROUP PARTS VRAM 4G MICRON X7695138010 X76_VRAM_MIC_4G@
OVRM	ZZZ ALT. GROUP PARTS OVRM IC ON HLXA4 X7695138011 X76_OVRM_ON@	ZZZ ALT. GROUP PARTS OVRM IC UPI HLXA4 X7695138012 X76_OVRM_UPI@

Screw Hole



LASER BARCODE

CODE1 @
BARCODE_8X8

CODE2 @
BARCODE_12X4

CODE3 @
BARCODE_20X4

DAZ

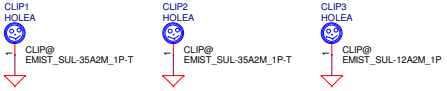
ZZZ
HLXA4 LA-L931P LS-L931P/K053P
DAZ3SD00101
DAZ_HLXA4@

ZZZ
HLXA5 LA-L931P LS-L932P/K057P
DAZ3SE00101
DAZ_HLXA5@

ZZZ
HLXC4 LA-L931P LS-L933P/L934P
DAZ3TI00101
DAZ_HLXC4@

Fiducial Mark

Clip



	HLXA4	HLXA5	HLXC4
X4E	ZZZ SMT EMC DIS GN18 EE HLXA4 X4EAUH38L02 14_X4E_DIS18@ ZZZ SMT EMC UMA EE HLXA4 X4EAUH38L01 14_X4E_UMA@ ZZZ SMT EMC DIS GN20 EE HLXA4 X4EAUH38L03 14_X4E_DIS20@	ZZZ SMT EMC DIS GN18 LAL931 HLXA5 X4EAUH38L54 15_X4E_DIS18@ ZZZ SMT EMC UMA FOR EE HLXA5 X4EAUH38L53 15_X4E_UMA@ ZZZ SMT EMC DIS GN20 FOR EE LAL931 HLXA5 X4EAUH38L55 15_X4E_DIS20@	ZZZ SMT EMC UMA FOR EE HLXC4 X4EAUH38LA1 YOGA_X4E@

Crystal
ZZZ ALT. GROUP PARTS XSTAL 32.768 3215 HLXA4 X7695138013 X76_Crystal_32_3215@ ZZZ ALT. GROUP PARTS XSTAL 32.768 2012 HLXA4 X7695138014 X76_Crystal_32_2012@

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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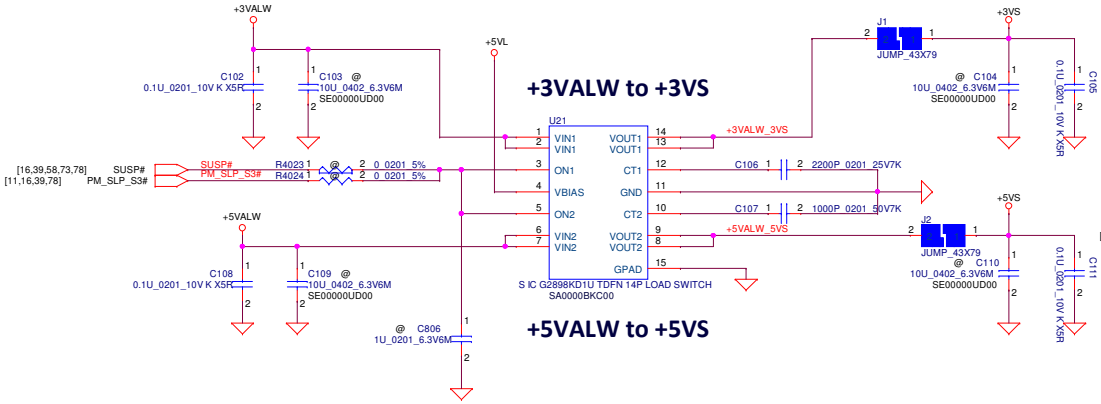
Compal Electronics, Inc.

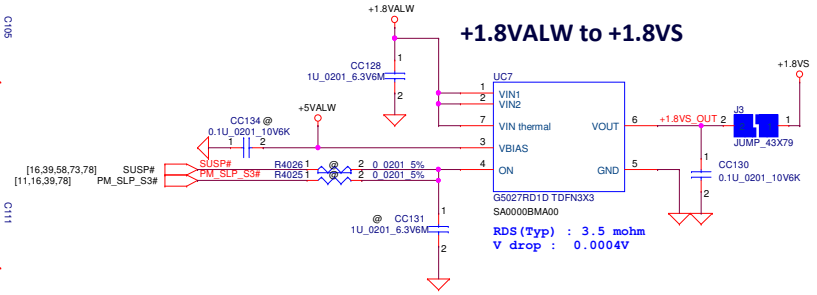
Title: PWRBTN/ FAN / Screws_EE

Size | Document Number: LA-L931P | Rev: 1.0

Date: Wednesday, August 31, 2022 | Sheet 77 of 120

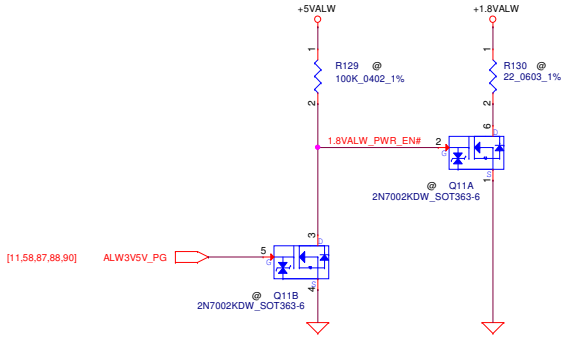
DC to DC





DISCHARGE CIRCUIT

For +1.8VALW Discharge



Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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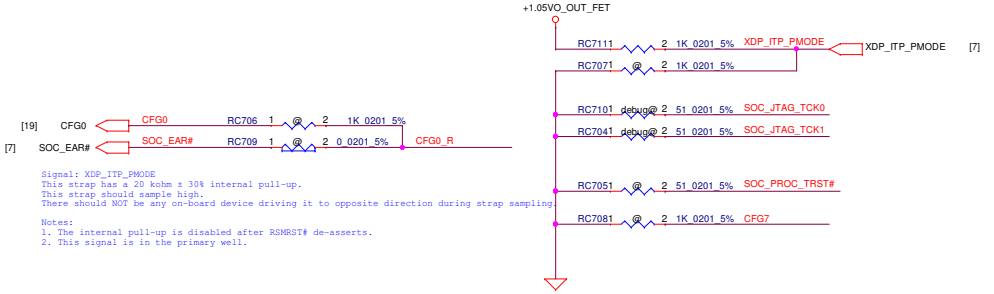
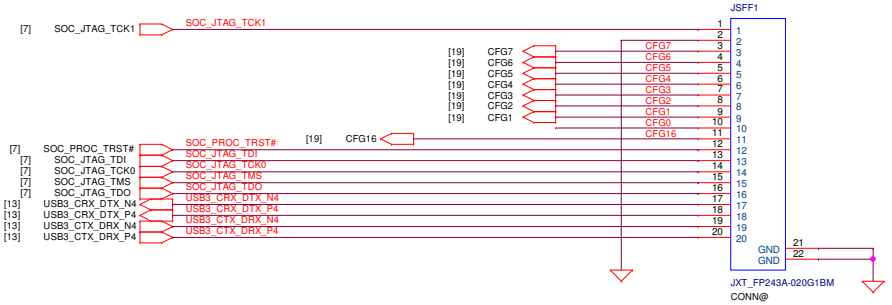
Compal Electronics, Inc.			
Title	DC Interface & Sequence Logic EE		
Size	Document Number		Rev
	LA-L931P		1.0
Date:	Thursday, March 31, 2022	Sheet	78 of 120



To DEBUG CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: XDP/CMC/APS Debug Conn EE

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 Sheet 79 of 120

Security Classification	Compal Secret Data		
Issued Date	2021/10/12	Deciphered Date	2021/10/12

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Compal Electronics, Inc.

Title: **FIP Conn EE**

Size	Document Number	Rev
	LA-L931P	1.0

Date: Tuesday, January 25, 2022 | Sheet 80 of 120

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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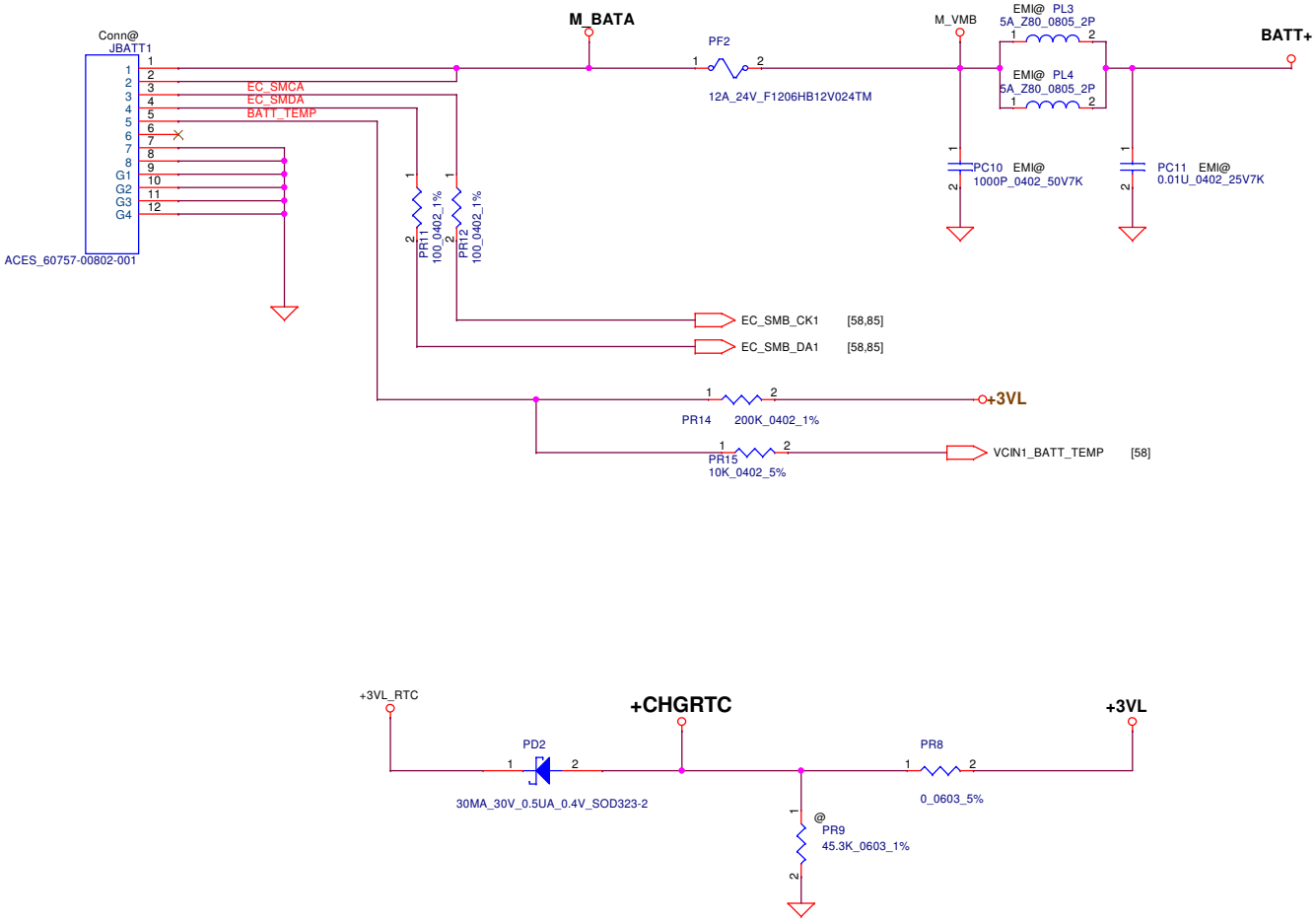
Compal Electronics, Inc.

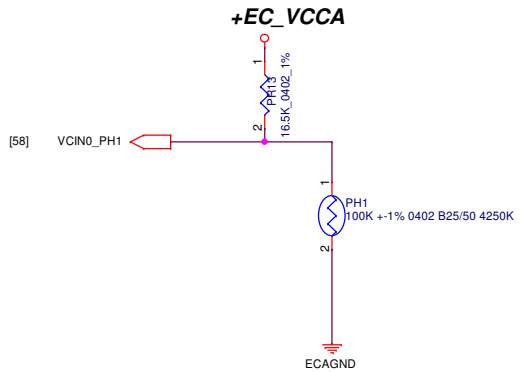
Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 81 of 119



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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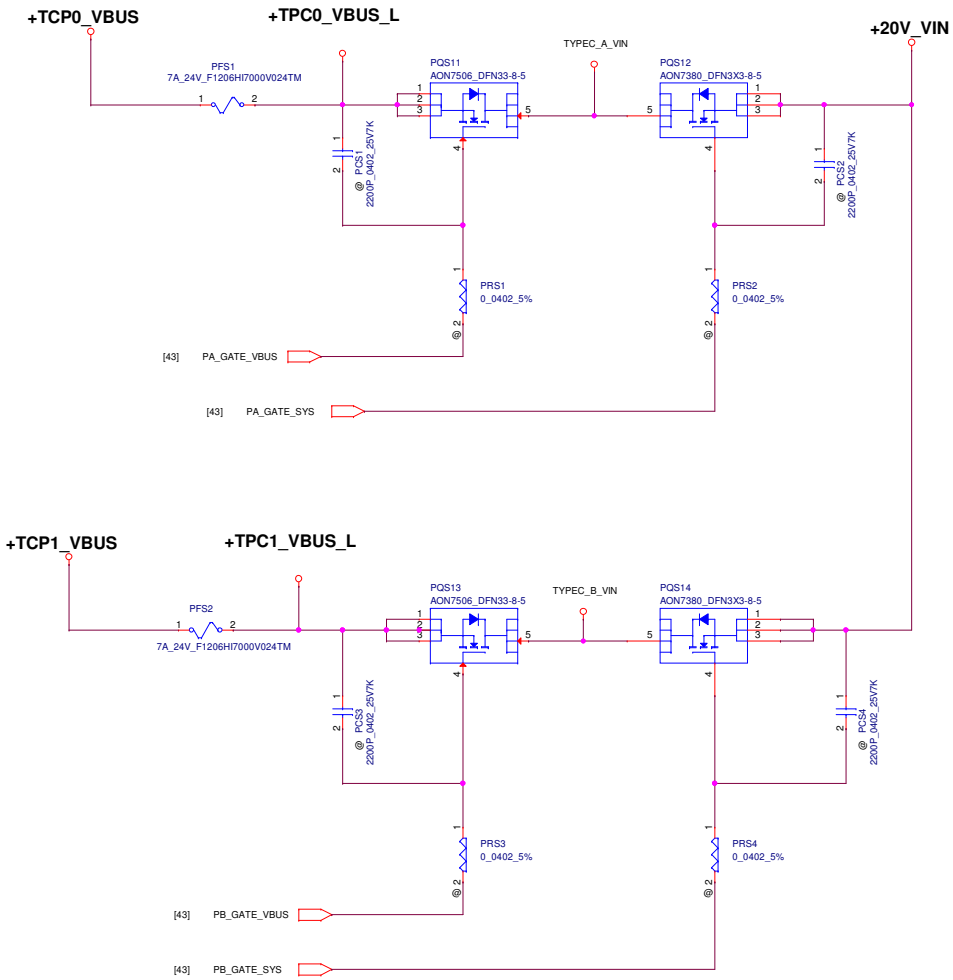
Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP/RTC**

Size	Document Number	Rev
Custom	LA-K051P	1.0

Date: Wednesday, March 02, 2022 Sheet 82 of 119



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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: **PWR- DC Conn/Type-C PD in**

Size	Document Number	Rev
Custom	LA-K051P	1.0

Date: Wednesday, March 02, 2022 | Sheet 83 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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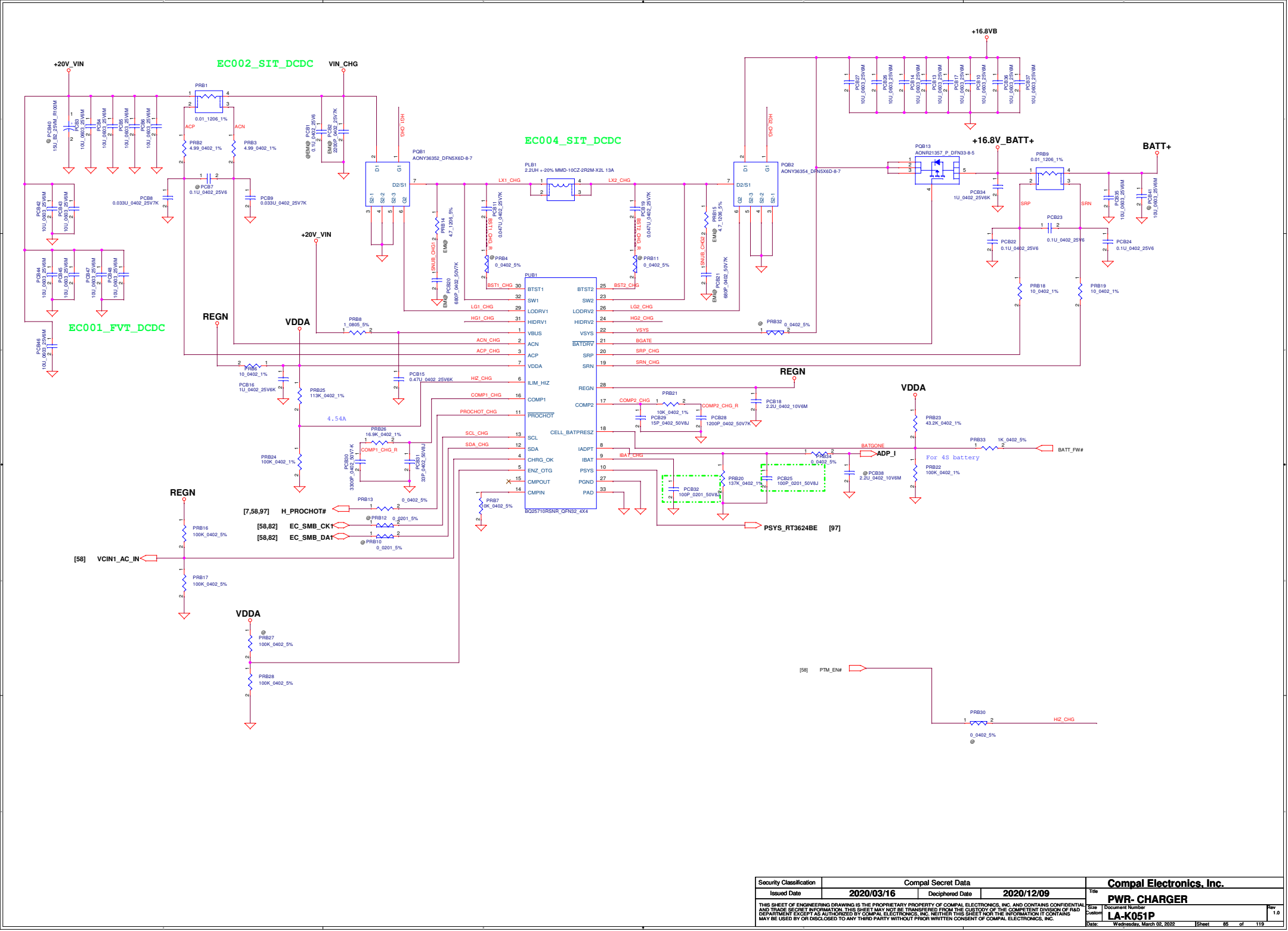
Compal Electronics, Inc.

Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 84 of 119



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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: **PWR- CHARGER**

Size: Custom | Document Number: **LA-K051P** | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 85 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

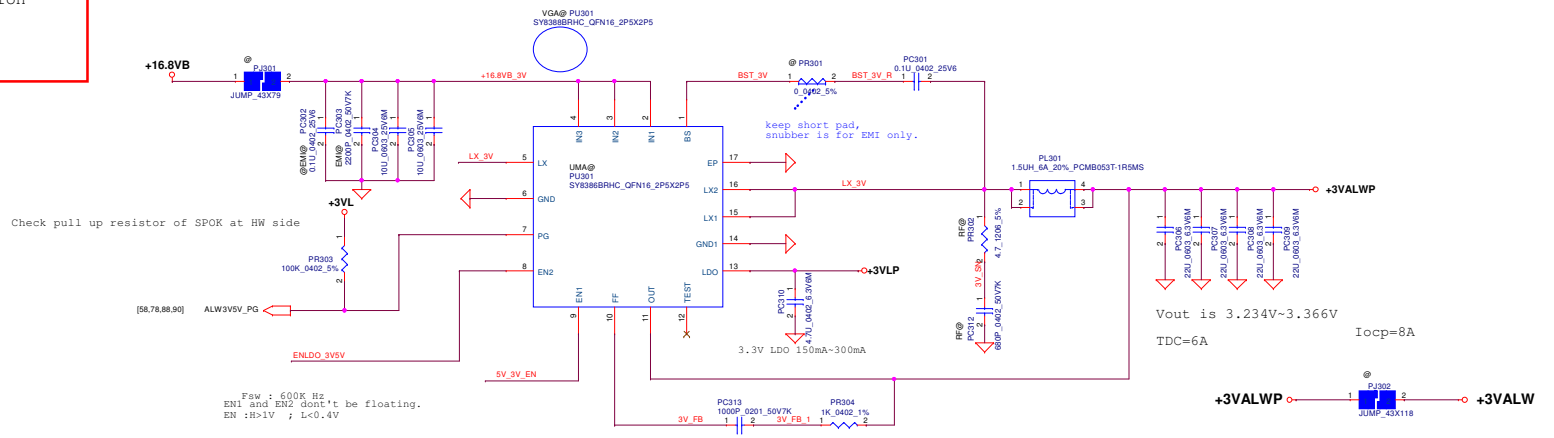
Title: **PWR- Reserve**

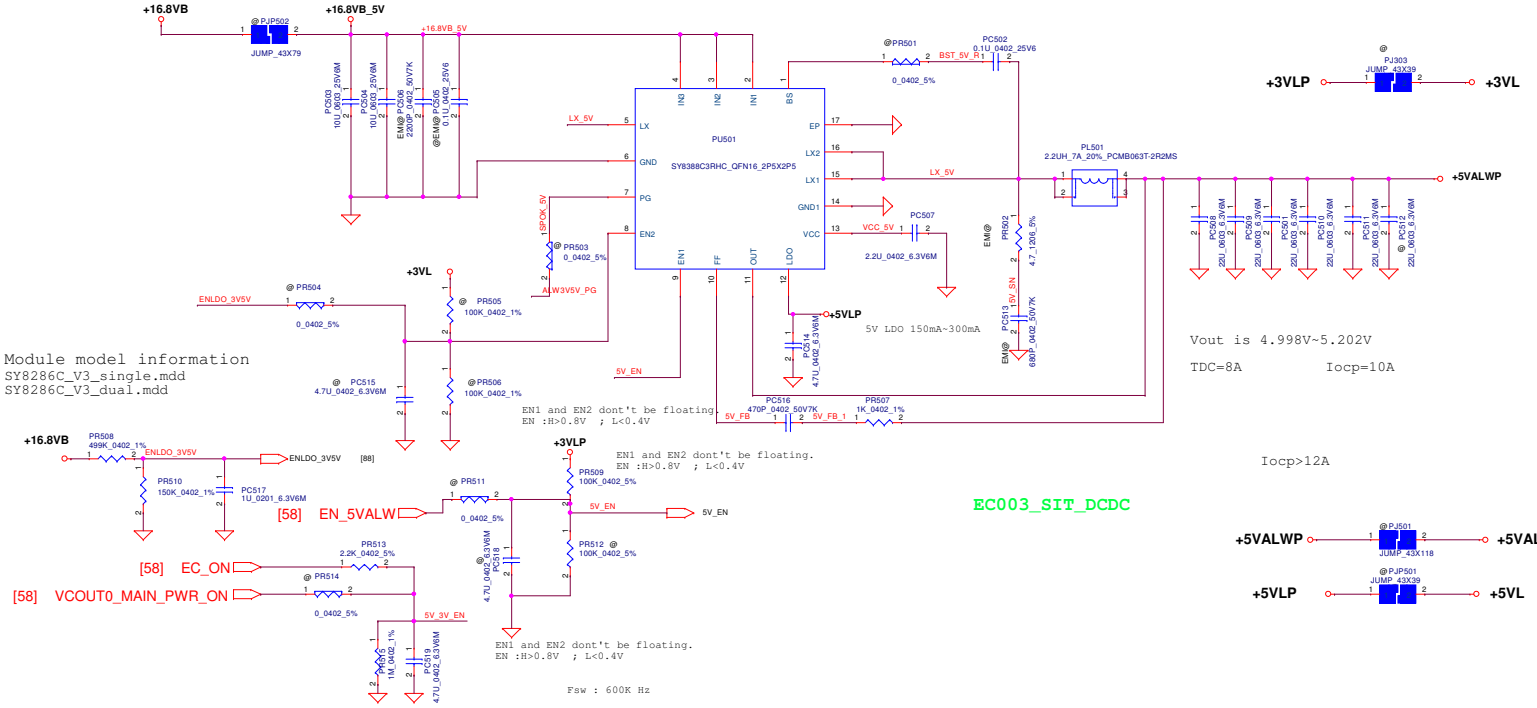
Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 86 of 119

Module model information

SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd





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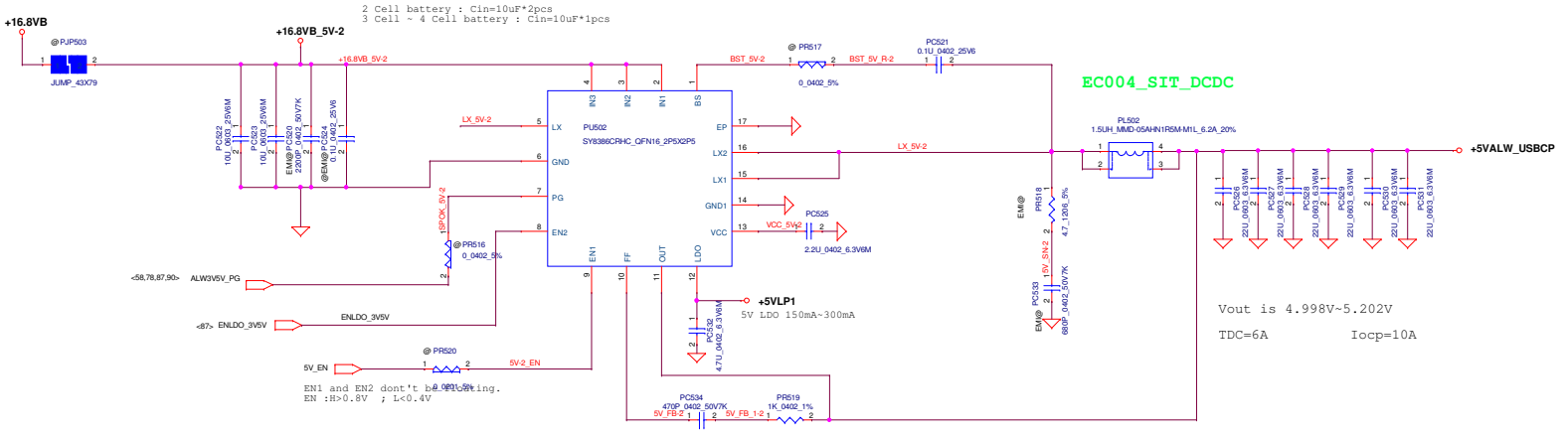
Title: PWR- 3VALW/5VALW1

Size: Custom | Document Number | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 87 of 119



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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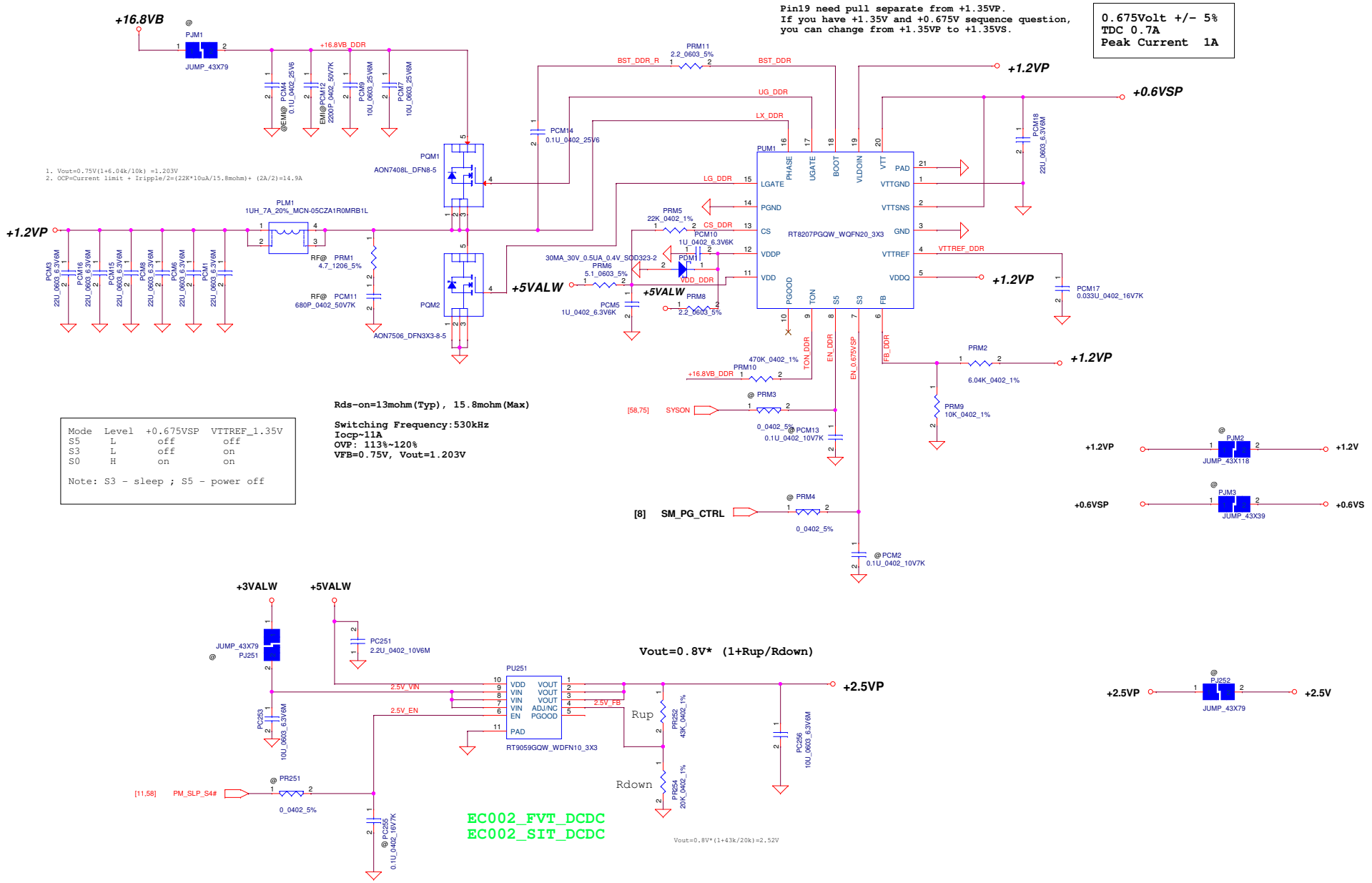
Compal Electronics, Inc.			
Title	P88-PWR-5VALW_USBC		
Size	Document Number		Rev 1.0
Date: Wednesday, March 02, 2022	Sheet 88	of	119



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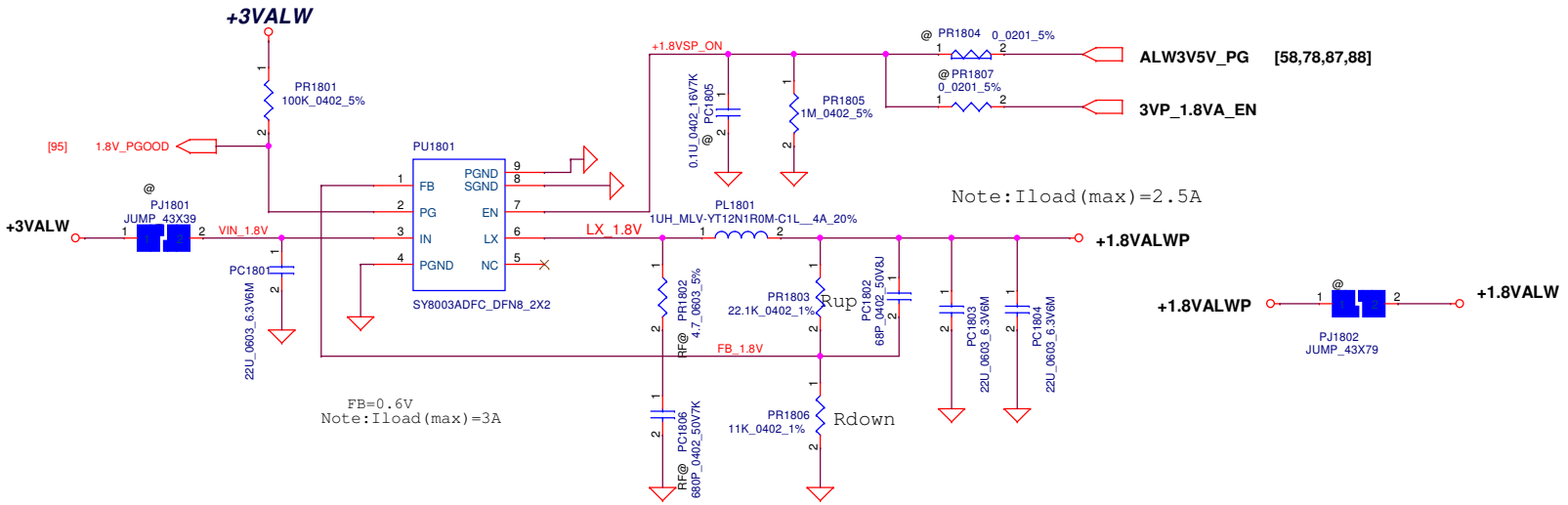
Compal Electronics, Inc.

Title: **PWR- DDR**

Size: Custom | Document Number: **LA-K051P** | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 89 of 119



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: **PWR- 1.8VALWP**

Size: Custom | Document Number: **LA-K051P** | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 90 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 91 of 119

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 92 of 119

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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 93 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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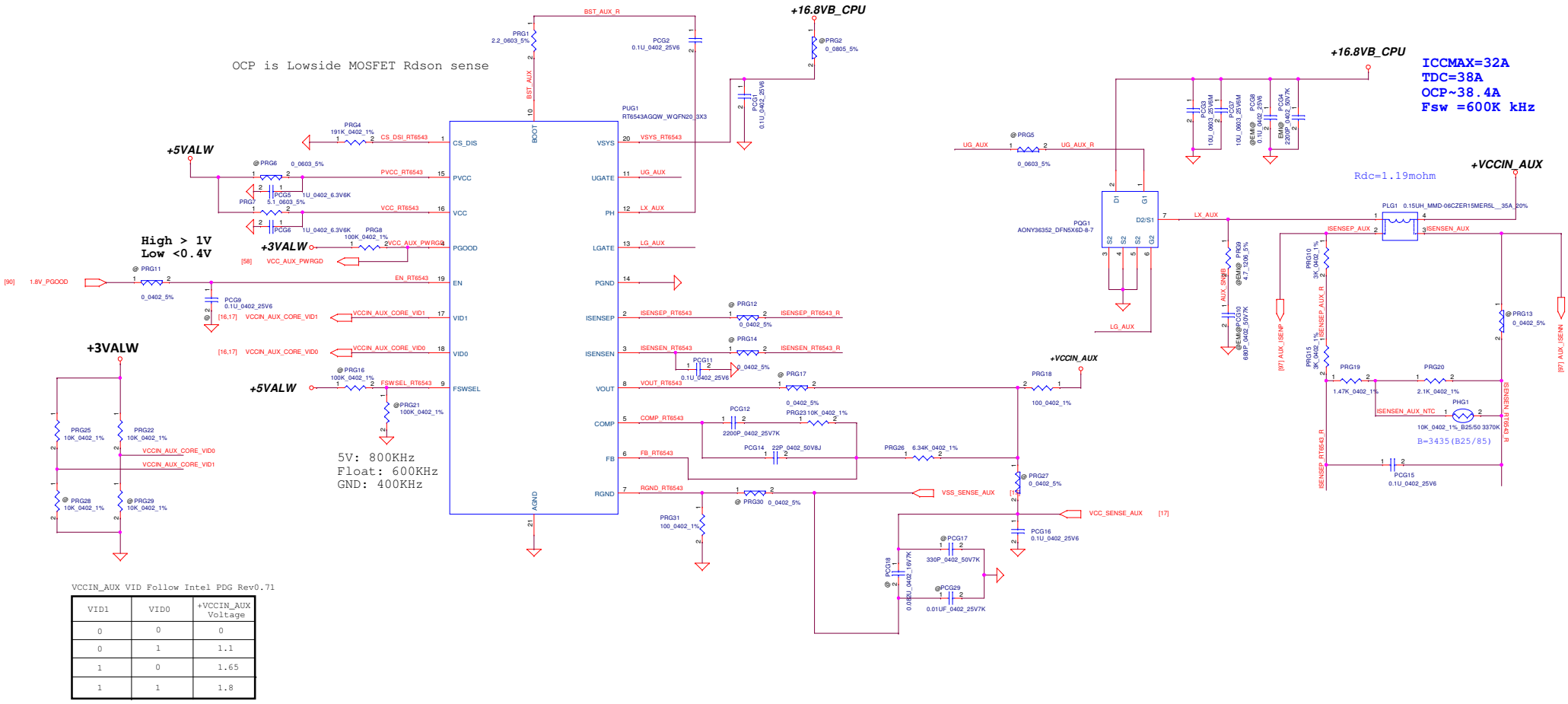
Compal Electronics, Inc.

Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 94 of 119



VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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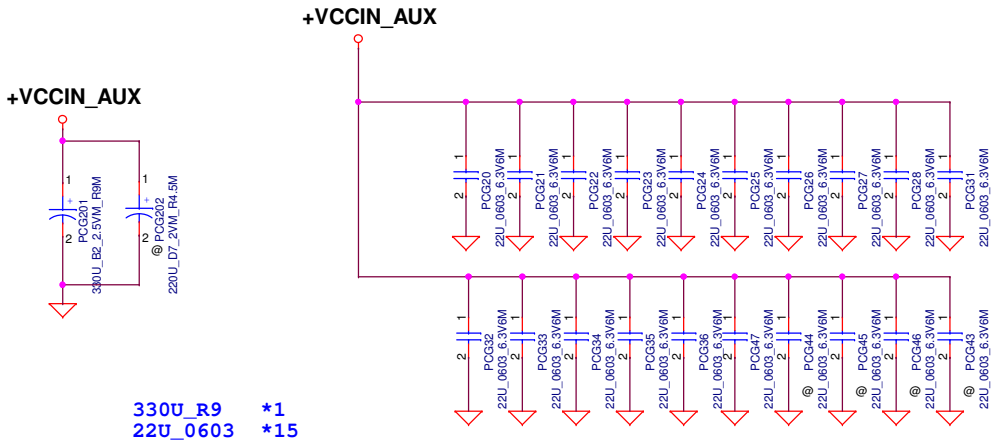
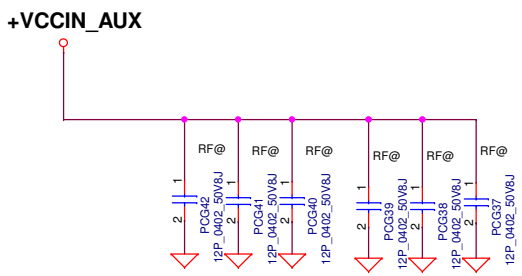
Compal Electronics, Inc.			
Title	PWR- VCCIN_AUX(MP2941)		
Size: Custom	Document Number: LA-K051P		Rev: 1.0
Date: Wednesday, March 02, 2022	Sheet 95 of 119		





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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: PWR- VCORE Cap

Size	Document Number	Rev
Custom	LA-K051P	1.0

Date: Wednesday, March 02, 2022 Sheet 96 of 119

ADL-P_28W

+VCC_CORE

ICCMAX=80A
TDC=47A
OCP=96A
DC LL=2.3m ohm

Switching Freqency= 600K Hz

+VCC_GT

ICCMAX=40A
TDC=23A
OCP=48A
DC LL=3.2m ohm

ADL-P_15W

+VCC_CORE

ICCMAX=60A
TDC=32A
OCP=72A
DC LL=2.8m ohm

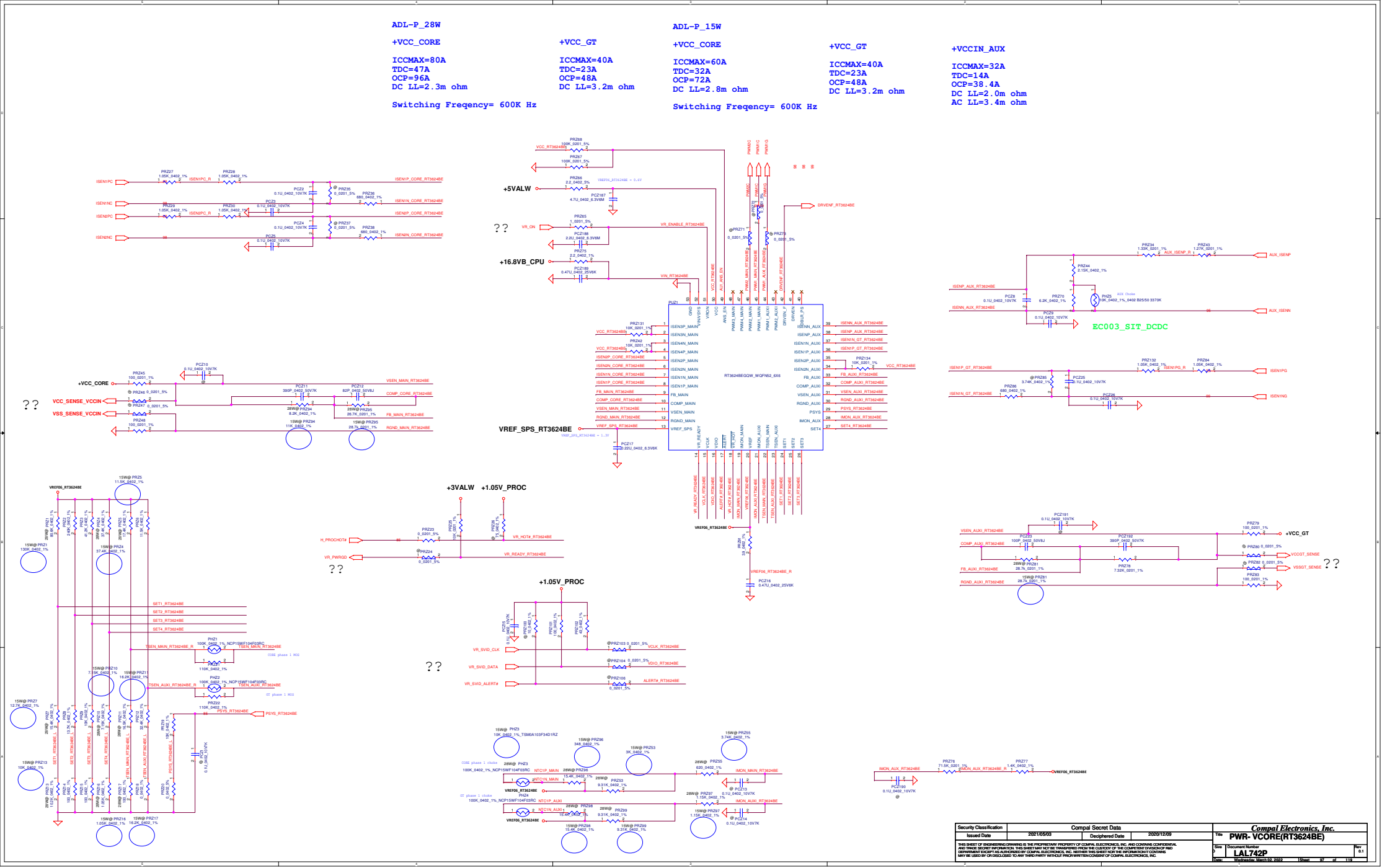
Switching Freqency= 600K Hz

+VCC_GT

ICCMAX=40A
TDC=23A
OCP=48A
DC LL=3.2m ohm

+VCCIN_AUX

ICCMAX=32A
TDC=14A
OCP=38.4A
DC LL=2.0m ohm
AC LL=3.4m ohm



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2021/05/03	Deciphered Date	2020/12/09	Title: PWR- VCORE(RT3624BE)
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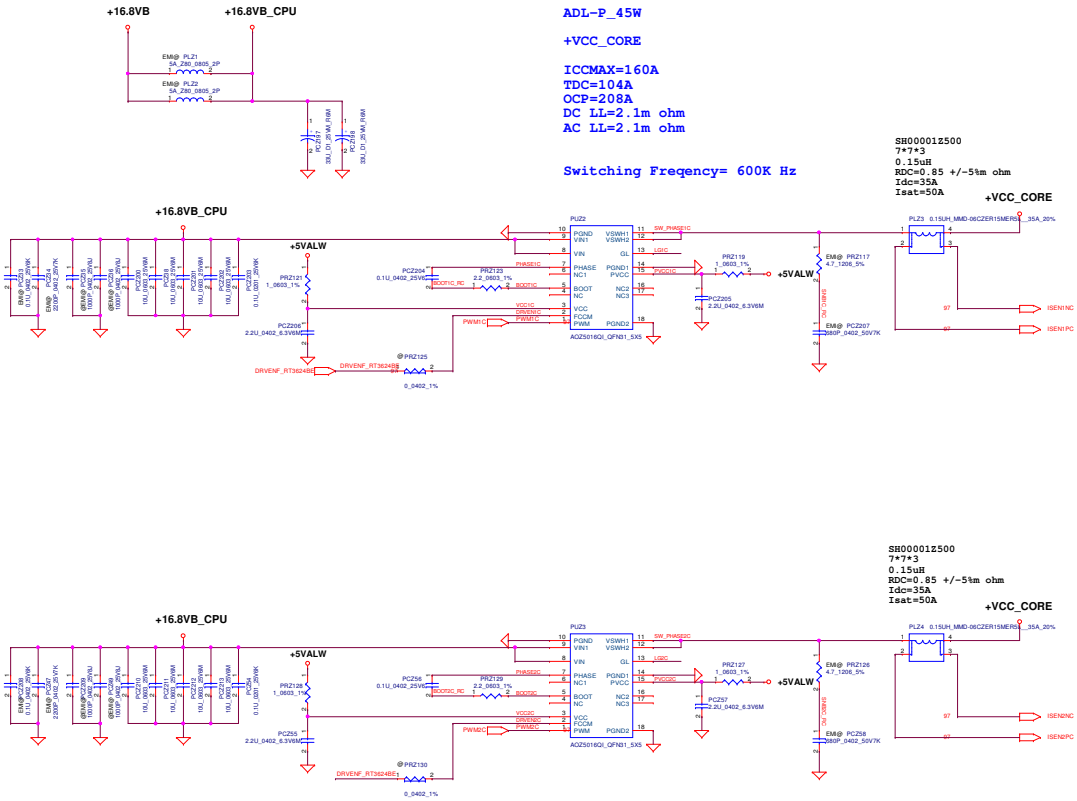
			Date: Wednesday, March 02, 2022	Sheet 97 of 119



ZCD:
SiC631= DRVEN
SiC632= DRVEN
SiC634= DRVEN
AOZ5038= DRVEN
FDMF3035= DRVEN
FDMF3037= DRVEN
FDMF5823= HighTHWn:
SiC631= Floating
SiC632= High
SiC634= Floating
AOZ5038= Floating
FDMF3035= Floating
FDMF3037= Floating
FDMF5823= High
DBL# :
SiC631= Floating
SiC632= High
SiC634= Floating
AOZ5038= Floating
FDMF3035= Floating
FDMF3037= Floating
FDMF5823= DRVEN

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: PWR- VCORE SW

Size	Document Number	Rev
2	LA-K051P	1.0

Date: Wednesday, March 02, 2022 | Sheet 38 of 119

ADL-P_15/28W

+16.8VB

+16.8VB_CPUGT

EMI@ PLG5
5A_Z80_0805_2P

+VCC_GT

ICCMAX=40A
TDC=23A
OCP=48A
DC LL=3.2m ohm

Common part
7*7*3
0.1uH
RDC=0.9 +/-5%m ohm
Idc=35A
Isat=41A

+16.8VB_CPUGT

+5VALW

PUG2
AOZ5016QI_QFN31_5X5

PRG40 1_0603_1%
PCG60 2.2U_0402_6.3V6M
DRVENF_RT3624BE
@PRG48 0_0402_1%
PWM1G
PCG61 0.1U_0402_25V6
PRG41 2.2_0603_1%
BOOT1_RC_GT
PHASE1_GT
VCC1_GT
DRVEN1_GT
SW_PHASE1_GT
LG1_GT
PVCC1_GT
PRG42 1_0603_1%
PCG62 2.2U_0402_6.3V6M
+5VALW
EMI@ PRG43 4.7_1206_5%
SNB1_RC_GT
PCG63 680P_0402_50V7K
PLG6 0.15UH_MMD-06CZER15MER5_35A_20%
ISEN1NG
ISEN1PG

EMI@ PCG71 0.1U_0402_25V6K
EMI@ PCG72 2200P_0402_25V7K
@EMI@ PCG73 1000P_0402_25V8J
@EMI@ PCG74 1000P_0402_25V8J
PCG75 10U_0603_25V6M
PCG76 10U_0603_25V6M
@ PCG77 10U_0603_25V6M
@ PCG78 10U_0603_25V6M
PCG79 0.1U_0201_25V6K

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Compal Electronics, Inc.

Title: **PWR-DR MOS GT**

Size: Custom | Document Number: **LA-K051P** | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 99 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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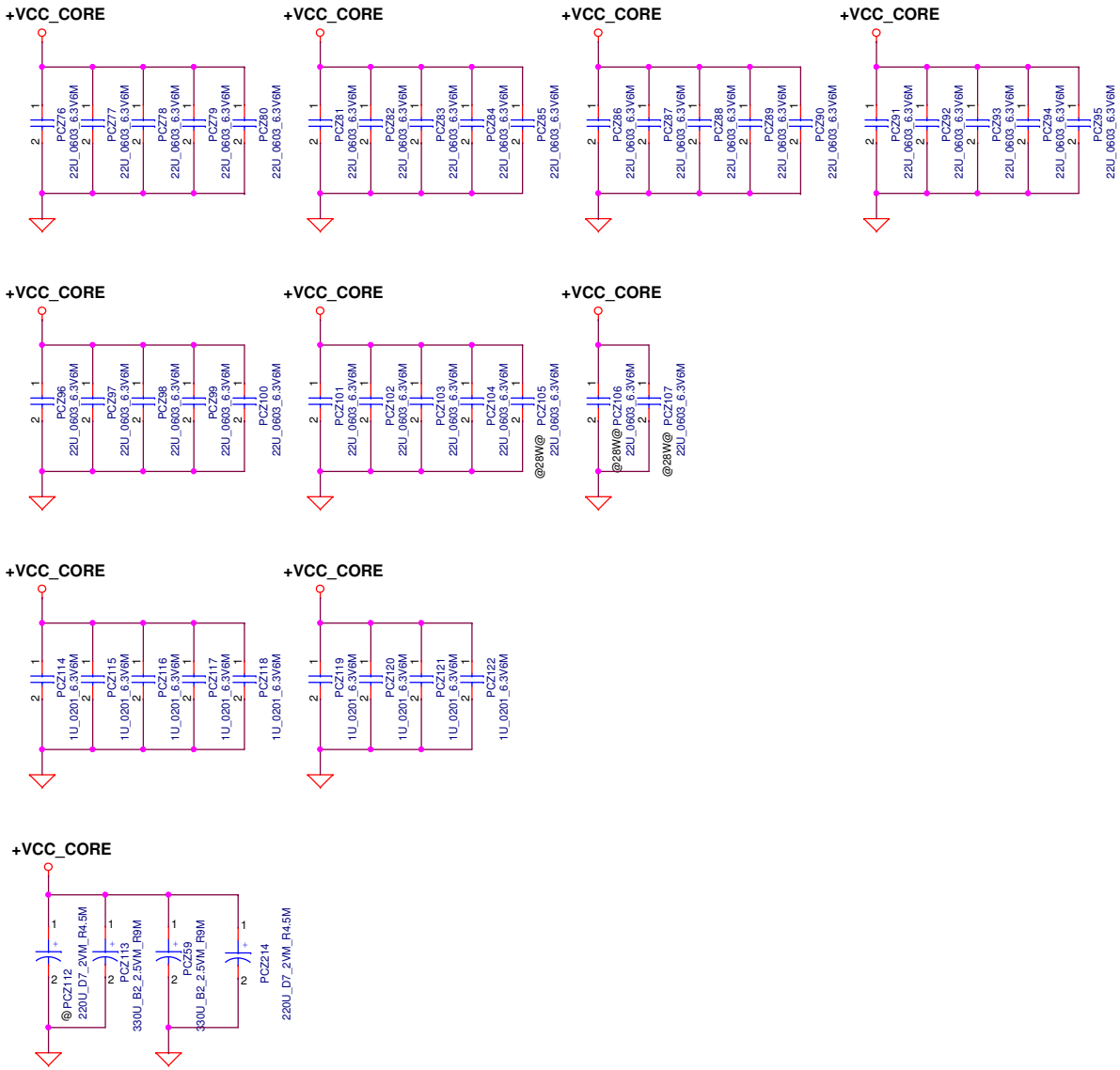
Compal Electronics, Inc.

Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 100 of 119



EC003_FVT_DCDC

EC006_SIT_DCDC

Intel ADL-P
+VCC_CORE Output CAP :

CPU 3phase:
330uF_D2 *2pcs(P98)
22uF_0603 *36pcs(32pcs上件，4pcs預留)
1uF_0201 * 9pcs

CPU 2phase:
330uF * 2pcs(P98)
22uF_0603 *36pcs(18pcs上件，18pcs預留)
1uF_0201 * 9pcs

Function feild:
CPU output cap:36.4

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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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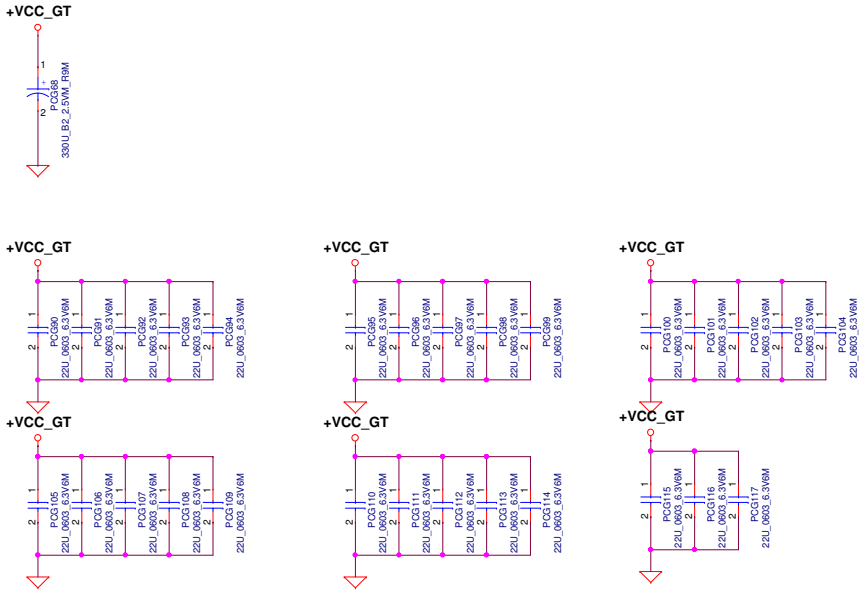
Compal Electronics, Inc.

Title: PWR- VCORE Cap

Size: Custom | Document Number: LA-K051P | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 101 of 119



Intel ADL-P
+VCC_GT Output CAP :

VCCGT 2phase:
330uF_D2 *1pcs(P99)
22uF_0603 *32pcs(28pcs上件，4pcs預留)

VCCGT 1phase:
330uF * 1pcs(P99)
22uF_0603 *32pcs(18pcs上件，14pcs預留)

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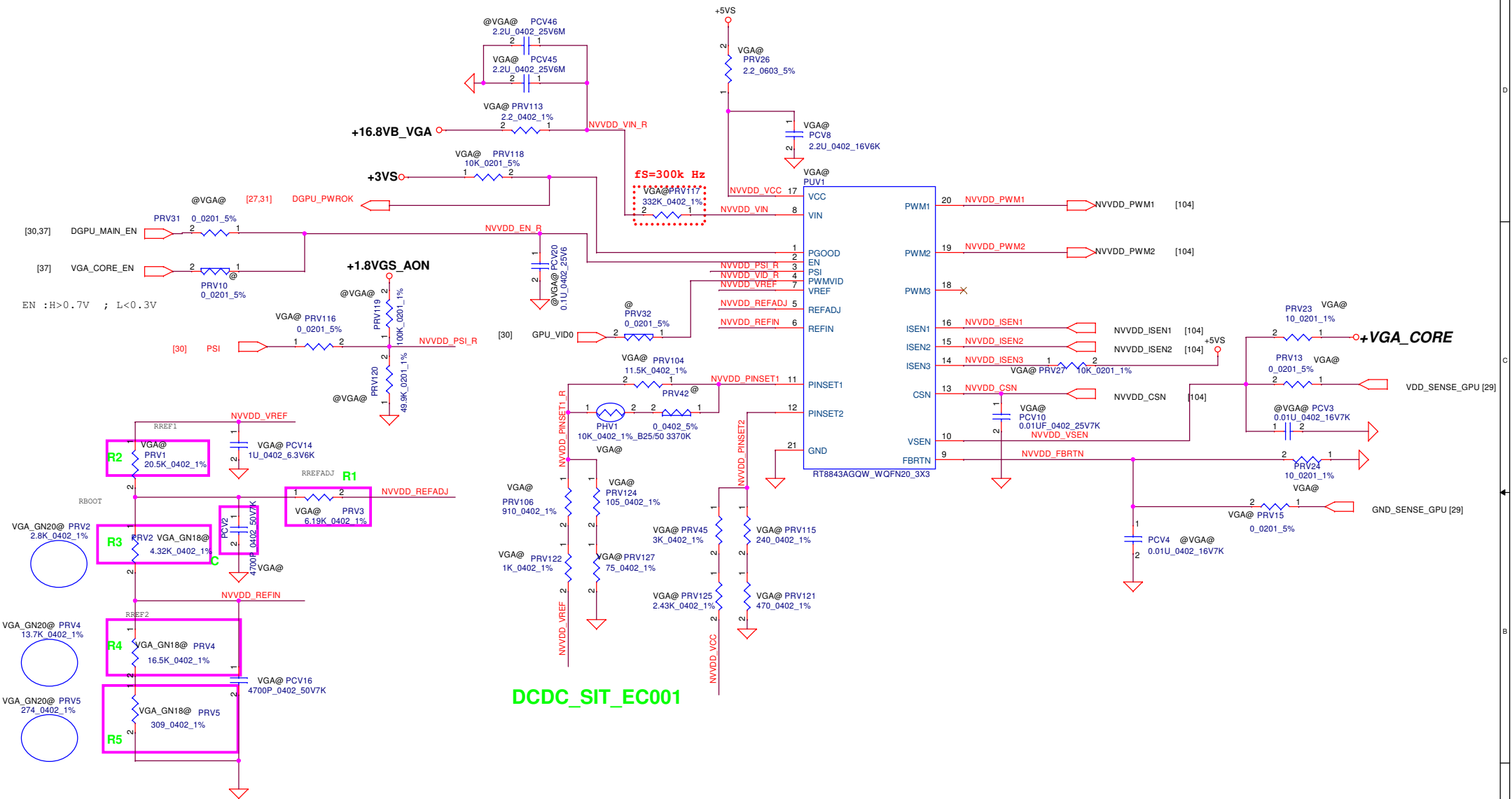
Compal Electronics, Inc.

Title: PWR-Decoupling_VCC_GT

Size: Custom | Document Number: LA-K051P | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 102 of 119



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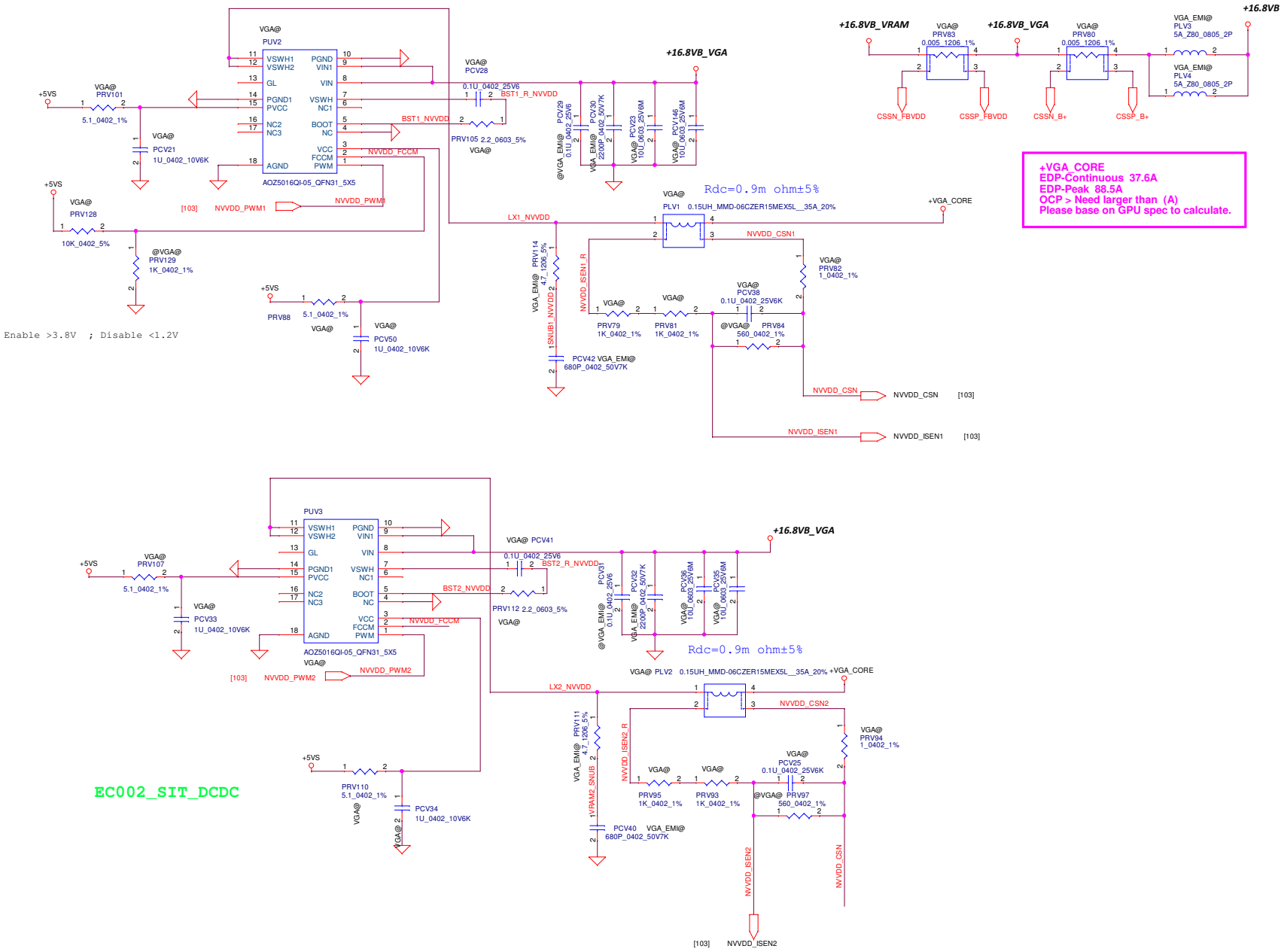
Compal Electronics, Inc.

Title: **PWR- GPU_CORE**

Size	Document Number	Rev
Custom	LA-K051P	1.0

Date: Wednesday, March 02, 2022 | Sheet 103 of 119



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Compal Electronics, Inc.

Title: **PWR- GPU_CORE_SW**

Size	Document Number	Rev
Custom	LA-K051P	1.0

Date: Wednesday, March 02, 2022 Sheet 104 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 105 of 119

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Issued Date	2020/03/16	Deciphered Date	2020/12/09

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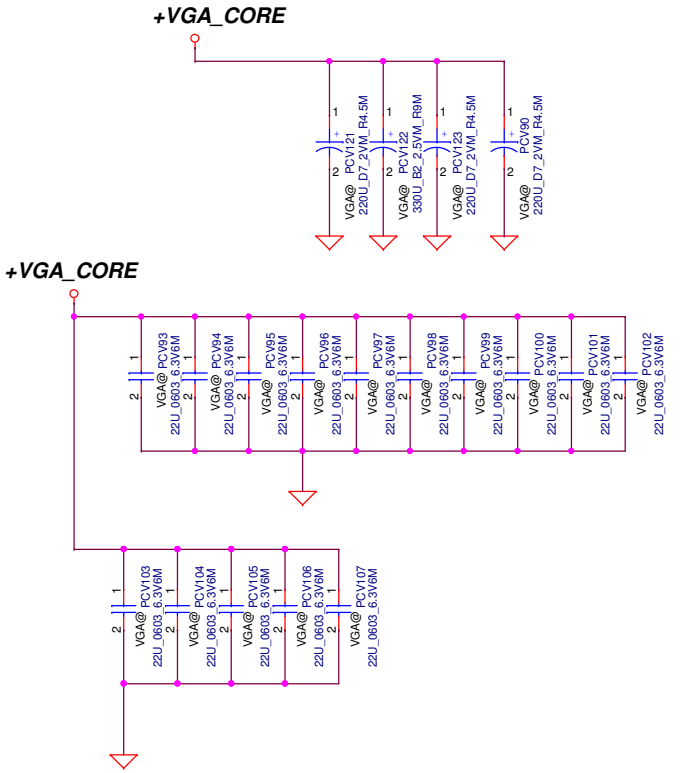
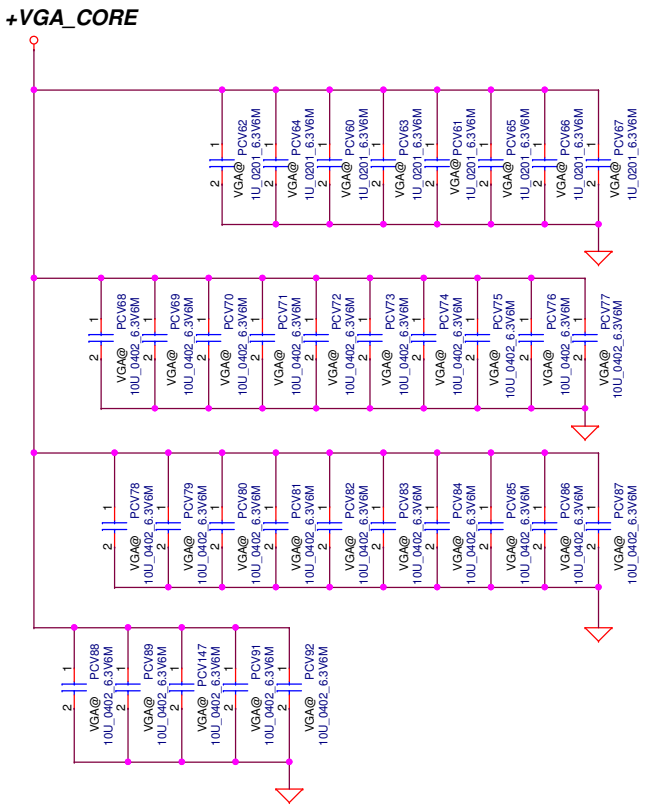
Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 106 of 119





VGA_CORE output cap

330U_B2_2.5V 1pcs

220U_D7_2.5V 3pcs

22U_0603_6.3V 10pcs

10U_0603_6.3V 12pcs

1U_0402_16V 5pcs

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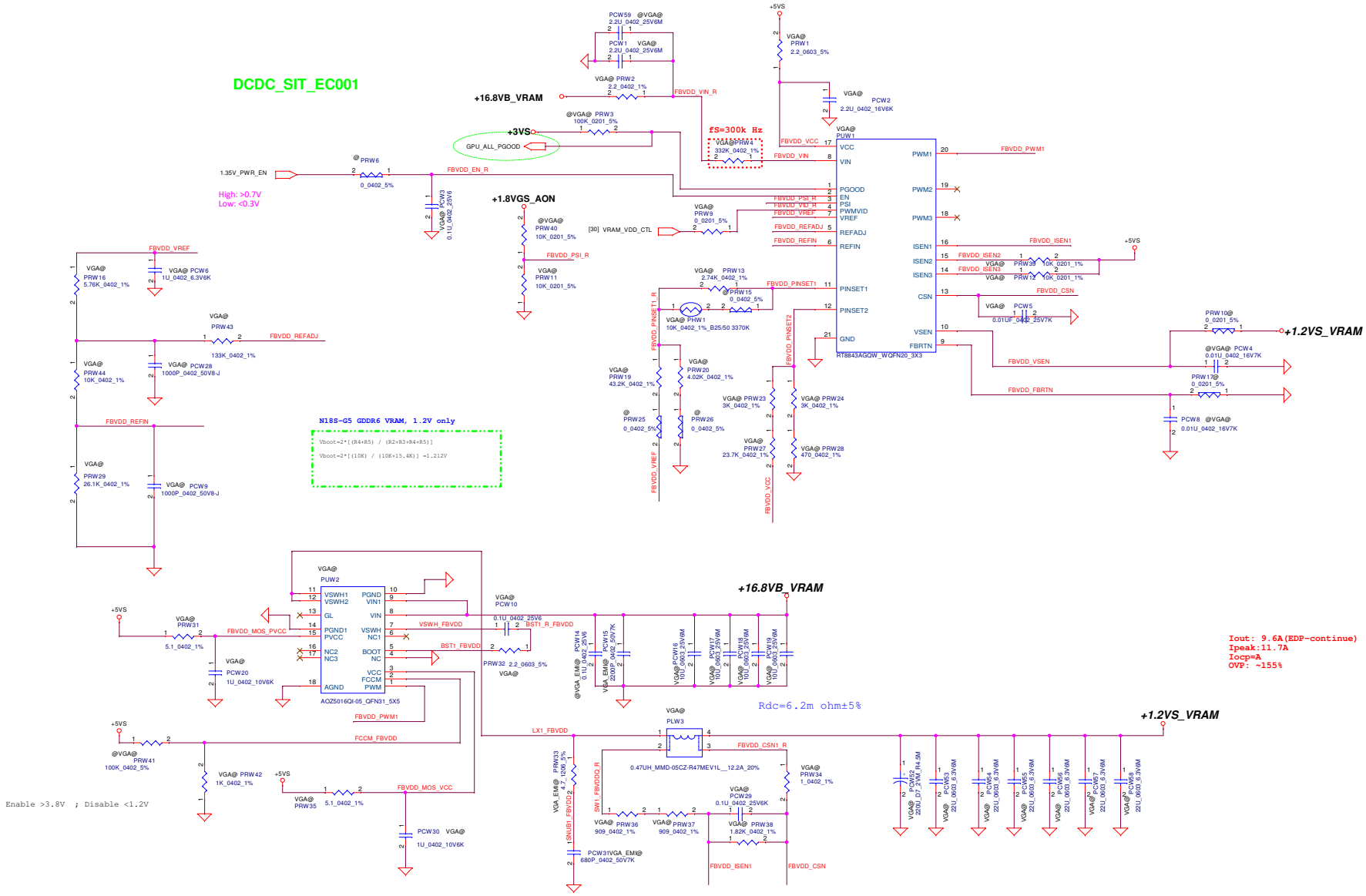
Compal Electronics, Inc.

Title: PWR- GPU_CORE Cap

Size: Custom | Document Number: LA-K051P | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 107 of 119



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Size: Custom	Document Number: LA-K051P
Rev	1.0
Date: Wednesday, March 02, 2022	Sheet 106 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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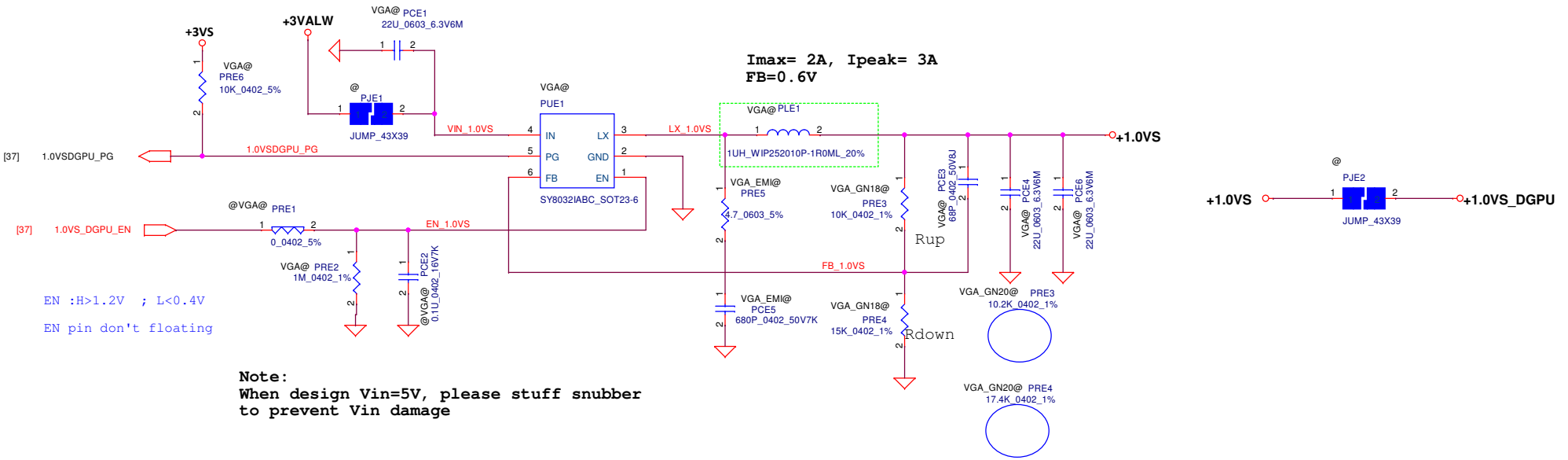
Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 109 of 119



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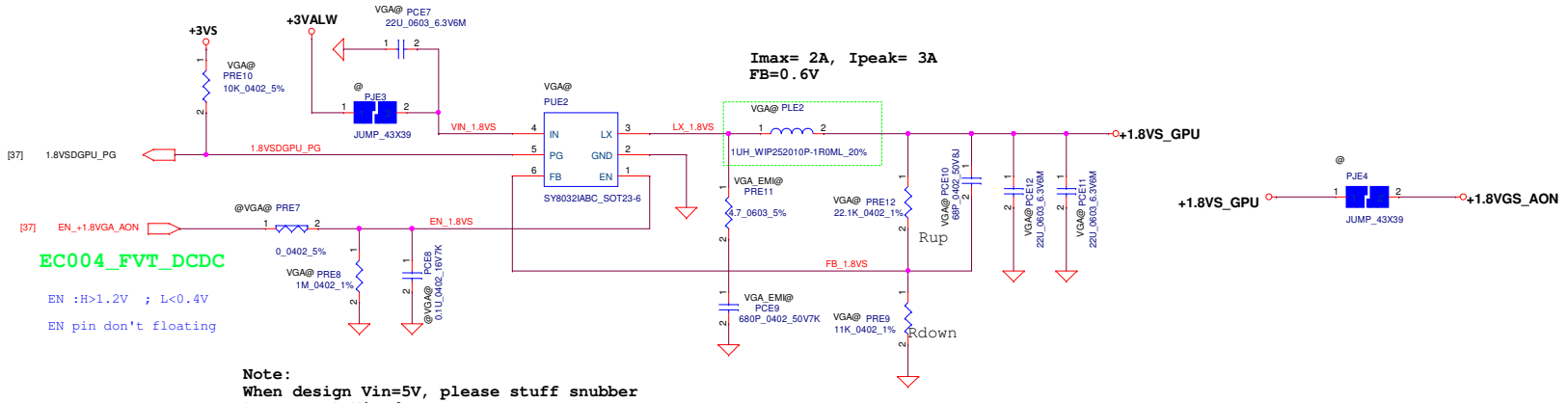
Compal Electronics, Inc.

Title: PWR- GPU 1.0V

Size: Custom | Document Number: LA-K051P | Rev: 1.0

Date: Wednesday, March 02, 2022 | Sheet 110 of 119



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Title	PWR- Reserve		
Size: Custom	Document Number: LA-K051P		Rev: 1.0
Date: Wednesday, March 02, 2022	Sheet 111 of 119		

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Title: **PWR- Reserve**

Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 112 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 113 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 114 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 115 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 116 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 117 of 119

Security Classification	Compal Secret Data		
Issued Date	2020/03/16	Deciphered Date	2020/12/09

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Size	Document Number	Rev
Custom	**LA-K051P**	1.0

Date: Wednesday, March 02, 2022 | Sheet 118 of 119